Announcement

As planned, a test will be given on Thursday, Nov. 12, 2015, in class. The test will cover Chapter 3. A review will be given on Thursday, Nov. 5.

Homework Assignment # 5

(1) For the circuit schematic shown in Fig. 1, do the following:

(a) Derive the next state logic function;

(b) Derive the output function for $Z$;

(c) Obtain the combined state transition and output table of this circuit;

(d) Obtain the state transition diagram of this circuit.

(2) Design a circuit that recognizes the occurrence of a particular sequence of bits, regardless of where it occurs in a longer sequence. This “sequence recognizer” has one input $X$ and one output $Z$. It has reset applied to the direct reset inputs on its $D$ flip-flops to initialize the state of the
circuit to all zeros. The circuit is to recognize the occurrence of the sequence of bits 1101 on $X$ by making $Z$ equal to 1 when the previous 3 inputs to the circuit were 110 and current input is a 1. Otherwise, $Z$ equal to 0.

(a) Give a state transition diagram;

(b) Give a combined state transition and output table;

(c) Give a state coding;

(d) Based on (a), (b) and (c), give simplified (if possible) Boolean equations for the next state and output logic;

(e) Give the circuit schematic based on (d).

Due:

Turn in your work on Thursday, Nov. 5, 2015.