Random Access Memory (RAM)

A word is an entity of bits that moves in and out of memory as a unit. If for a memory the access time takes the same time regardless of the location, the memory is called random access memory.

![Block Diagram of Memory](image)

**FIGURE 8-1**
Block Diagram of Memory

<table>
<thead>
<tr>
<th>Memory Address</th>
<th>Memory Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Binary</strong></td>
<td><strong>Decimal</strong></td>
</tr>
<tr>
<td>0000000000</td>
<td>0</td>
</tr>
<tr>
<td>0000000001</td>
<td>1</td>
</tr>
<tr>
<td>0000000010</td>
<td>2</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>1111111101</td>
<td>1021</td>
</tr>
<tr>
<td>1111111110</td>
<td>1022</td>
</tr>
<tr>
<td>1111111111</td>
<td>1023</td>
</tr>
</tbody>
</table>

**FIGURE 8-2**
Contents of a 1024 × 16 Memory
Write and Read Operations

Write:

The steps that must be taken for a write are as follows:
1. Apply the binary address of the desired word to the address lines.
2. Apply the data bits that must be stored in memory to the data input lines.
3. Activate the Write input.

Read:

The steps that must be taken for a read are as follows:
1. Apply the binary address of the desired word to the address lines.
2. Activate the Read input.

Memory is made up of RAM chips, plus additional logic circuits.

Chip Select (CS) of a RAM chip is used to enable read/write operations on the chip.

□ TABLE 3-1
Control Inputs to a Memory Chip

<table>
<thead>
<tr>
<th>Chip Select CS</th>
<th>Read/Write R/W</th>
<th>Memory operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>×</td>
<td>None</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Write to selected word</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Read from selected word</td>
</tr>
</tbody>
</table>
Timing Waveforms

access time: maximum time from the application of address to the appearance of the data at data output.

write cycle time: maximum time from the application of address to the completion of storing a word.

For synchronization purpose, access time and write cycle time are rounded up to fixed numbers of clock periods (cycles).

---

Clock

Address

Memory enable

Read/Write

Data input

---

20 ns

Address valid

---

20 ns

Data valid

---

75 ns

write cycle time

(a) Write cycle

---

Clock

Address

Memory enable

Read/Write

Data output

---

65 ns

access time

(b) Read cycle
Integrated-Circuit (IC) RAM

Static RAM (SRAM)

The stored information remains valid as long as power is on.

Dynamic RAM (DRAM)

Information is stored in the form of electric charges on capacitors. The stored charge must be periodically recharged by refreshing the DRAM.

Comparison

DRAM: Reduced power consumption and larger storage capacity in a single chip.

SRAM: Easier to use, and faster.
Logic of a SRAM cell

![S-RAM Cell Diagram](image)

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Q̅</th>
<th>C</th>
<th>C̅(E)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>B</td>
<td>D</td>
<td>no change</td>
<td>Q</td>
<td>Q̅</td>
</tr>
<tr>
<td>1</td>
<td>B</td>
<td>D</td>
<td>=1</td>
<td>=0</td>
<td>1 1 0 0</td>
</tr>
<tr>
<td>1</td>
<td>B</td>
<td>D</td>
<td>=0</td>
<td>=1</td>
<td>0 1 0 1</td>
</tr>
<tr>
<td>1</td>
<td>B</td>
<td>D</td>
<td>=1</td>
<td>=1</td>
<td>undefined</td>
</tr>
</tbody>
</table>

Note: \( \overline{B} \) is changed to \( D \), since in operation \( B = \overline{B} = 0 \) is possible.

Also note that \( C \) and \( \overline{C} \) are not always complement to each other. We use \( E \) instead of \( \overline{C} \).
A bit slice is a set of RAM cells and associated circuitry for a single bit position of a set of RAM words.

(a) Logic diagram

□ FIGURE 8-5
RAM Bit Slice Model
Read a Selected Bit

(a) Logic diagram

FIGURE 8-5
RAM Bit Slice Model
Write into a Selected Bit

(a) Logic diagram

□ FIGURE 5-5
RAM Bit Slice Model
A 16 x 1 RAM Chip

16 words, each having 1 bit.

Chip Select = 1
Read or Write a selected word

Chip Select = 0
No read and write regardless of the application of word select signal
Coincident Selection

Multiple bit slices (2-dimensional bit array)
2 decoders for generating selection signals

16 x 1 RAM Chip

Address = 1001

Advantages: Reduced number of gates and circuit complexity.
Reduced access and write cycle times.

Diagram of a 16 x 1 RAM Using a 4 x 4 RAM Cell Array
8 words
2 bits/word
Array of RAM Chips

1. Increasing the number of words

\[ \text{FIGURE 8-9} \]
Symbol for a 64K \( \times \) 8 RAM Chip

\[ \text{FIGURE 8-10} \]
Block Diagram of a 256K \( \times \) 8 RAM
2) Increasing Word Length

![Block Diagram of a 64K×16 RAM]

Figure 8-11
Block Diagram of a 64K×16 RAM

3) Combination of 1 and 2

Construct a RAM of desired word length and desired number of words.