PROJECT #6
Final Project: Layout & Verification

Due: Wed Dec 10, 2014 (start of class)

Project Introduction
For this project you will take your Verilog code from project 2 and lay it out using the cells that you generated in your cell library.

Project Goals

1) Automatic placement and routing of your design using Cadence’s Encounter
2) Run DRC (design rule checker) and LVS (layout versus schematic)
3) Run PrimeTime on the final layout using the extracted netlist to ascertain the worst-case delay

Project Rules & Requirements

1) Use an output capacitance of 25fF for all your outputs when testing, and input slew rates of 65 ps. (for Primetime)
2) At least 2000 cells.

What To Turn In (points are deducted for anything missing)

1) A cover page containing all the following information.
   • Name, student number, “EE6325”, and project title
2) Formal Report detailing complete design process from start to finish. This is where you will do your best to convince us that you have a quality design and you thought through your design carefully. Your report must include, but is not limited to, the following:
   • Discuss tradeoffs
   • Clearly describe the function of your design
   • Describe in detail the total inputs and outputs
   • Detail the testing process and describe how you tested it
   • Do not exceed 20 pages! (points will be deducted!)

3) Output Waveforms of your original Verilog/VHDL code along with the waveforms from simulations of the actual layout
4) Print out of the complete layout with rulers clearly showing sizes
5) DRC and LVS reports
6) Primetime report to determine the best possible clock period and total power consumed.
7) A hardcopy of project report is required; no soft copies.
Project Flow and Tutorial Links:

1) You need to use Cadence virtuoso layout editor to create abstract views for your standard cells.
   • [http://utdallas.edu/~akshay.sridharan/index_files/Page7161.htm](http://utdallas.edu/~akshay.sridharan/index_files/Page7161.htm)

2) You then need to generate LEF files and prepare your design for Automatic Place and Route.
   • [http://utdallas.edu/~akshay.sridharan/index_files/Page7161.htm](http://utdallas.edu/~akshay.sridharan/index_files/Page7161.htm)

3) Run Encounter to Place and route your synthesized Verilog from project 5
   • [http://utdallas.edu/~akshay.sridharan/index_files/Page11248.htm](http://utdallas.edu/~akshay.sridharan/index_files/Page11248.htm)

4) Then import the routed design to cadence.
   • [http://utdallas.edu/~akshay.sridharan/index_files/Page1195.htm](http://utdallas.edu/~akshay.sridharan/index_files/Page1195.htm)

5) You then need to clear DRC
   • [http://utdallas.edu/~akshay.sridharan/index_files/Page8227.htm](http://utdallas.edu/~akshay.sridharan/index_files/Page8227.htm)

6) You then need to clear LVS.
   • [http://utdallas.edu/~akshay.sridharan/index_files/Page8227.htm](http://utdallas.edu/~akshay.sridharan/index_files/Page8227.htm)

7) Then Run Static Timing analysis using Primetime.
   • [http://utdallas.edu/~akshay.sridharan/index_files/Page11797.htm](http://utdallas.edu/~akshay.sridharan/index_files/Page11797.htm)

8) **Yes you are now done and you are a VLSI expert!!!**