EE 6325 VLSI Design

Project #5: D Flip-Flop

Due: Wed. 19 November 2014

Project Introduction
For this project you will be using the Cadence Design tools to design, layout and characterize a D-Flip-Flop.

Project Goals
1) Minimize diffusion breaks and cell width
2) Match the cell height to that of your cells in Project 4, given that the height of the pdiff must be 6 contacts and ndiff must be 2 contacts.

Project Rules & Requirements
1) Use exactly the DFF design shown in class (falling-edge triggered master-slave with asynchronous reset).
2) Input/output pins must lie on a grid (an integer multiple of the grid spacing)
3) Minimize the use of vertical metal2, and no horizontal metal2.
4) Minimize the use of horizontal poly runs
5) The input slew rate is 80ps (the slew rate, for this problem, is defined as the time for the input to go from low (.2 Vdd) to high (.8 Vdd) and vice versa).
6) Assume a 25fF load capacitance when simulating
7) The DFF cell has 4 pins: D, Clk, R (reset, active high) and one output pin (Q).
8) Characterize the DFF using Siliconsmart ACE.

What To Turn In (points are deducted for anything missing)
1) A cover page containing all the following information.
   • Name, student number, and project title
   • D Flip-Flop times: Tsu_dd, Tsu_opt, Thold, T_{clk->Q}, and tD
   • Clearly state your width and height on the front.
2) Please include a short report describing the following
   • how you found your D Flip-Flop times
   • how you came up with your layout
3) D Flip-Flop layout with rulers showing the dimensions of the cell.
   • Show the uniform distance of your pin grid
   • Show height & width of entire cell
4) Waveforms and explanation showing how you computed Tsu_dd, Tsu_opt, Thold, T_{clk->Q}, and tD.
5) Spice testing setup file (Don’t include any spice netlist)
6) A hardcopy of project report is required; no soft copies.

Grading Breakdown
1) Correct functionality 30%
2) Cell Area 25%
3) Number of M2 used 25%
4) Report 20%