Project Introduction

For this project you will use Synopsys to generate a mapped netlist based on the library of cells that we have provided. After running Synopsys, you will have a better idea of the complexity of your design as well as an exact cell count. This project will also give you a good idea of what cells you will be creating for your own library.

Project Description/Requirements

1) Work through the Synopsys tutorial.
2) From the tutorial you will open your Verilog code and create a netlist based on the library that we have provided.
3) Print out the report showing the total number of cells used for your design. The report will be generated by Synopsys.
4) Take the mapped verilog that you created and concatenate it with the header.v file that we have provided.
5) Test the code with any Verilog simulator and obtain graphical waves of the mapped verilog. (Yes you will need graphical waves for this one!)
6) Compare with your behavioral verilog and verify that both function the same.

NOTE: You are required to have at least 2000 cells for your design

Report Layout

1) A cover page containing name, student number, and project title.
2) Visual Waveforms showing state transitions from mapped Verilog along with the waveforms from the behavioral Verilog so it is obvious that the two are performing identical functions.
3) Report from Synopsys showing total amount of cells in project.
4) ** If you have changed designs completely, you will also need to turn in your behavioral Verilog code for your new design along with a description. (Font – Verdana Font Size Strictly- 8 )
5) No waveforms with black background; points deducted for not following format.
6) A hardcopy of project report is required (Do not include the structural Verilog code)
7) Only email the structural Verilog code to the TAs.

Grading Breakdown

50% Mapped (structural) Verilog has the correct functionality
25% Report clarity and content
25% Design complexity and size