PROJECT #2: 21b X 21b Multiplier Design

Due: Wednesday Aug. 6 (5:30p)

Project Introduction
This project will strengthen your understanding of multipliers (and adders). You must design a 21b X 21b multiplier, where the emphasis is on speed.

Project Rules & Requirements
1) Design in schematic form using the 130nm IBM process technology.
2) Assume that the input operands are positive.
3) Verify your design using Hspice.
4) Each output must drive a 15fF load.
5) Use Siliconsmart ACE to characterize your cells and find the power and delay from Primetime.
6) You must use Booth-2, you must use partial product compression, and you must use a carry propagate adder of some type.

Grading Criteria (Competitive)
1. Functionality (40% reduction if TA applies a vector that causes the multiplier to fail)
2. Delay vs. Power (25%); the TA will rank all designs based on delay (D). However if two designs have a similar delay but a substantial difference in power, the one with the lower power will be considered better.
3. Report clarity (15%)
4. Demo to the TA (20%)

Report includes at least the following:

1) A cover page containing all the following information.
   - Name, student number, “EE7325”, and project title
2) Show worst-case delays and power reports from Primetime.
3) Hierarchical schematic (only show each unique cell once)