Void-free filling of spin-on dielectric in 22 nm wide ultrahigh aspect ratio Si trenches

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The authors demonstrate fabrication of ultrahigh aspect ratio nanotrenches, made by nanoimprint lithography and dimension reduction, as test bed shallow trench isolation structures for the 22 nm semiconductor node. Polysilazane based spin-on dielectric (SOD) material is spin coated into the nanotrenches, of 22 nm width and aspect ratio over 30, to evaluate gap filling property. Fourier transform infrared spectroscopy analysis is used to characterize the curing properties of the SOD, showing that the material can be cured in oxygen at temperatures of 600 °C and higher. Transmission electron microscopy images indicate that the filling is complete and void-free along the entirety of the trench. © *2009 American Vacuum Society.* [DOI: 10.1116/1.3244626]

I. INTRODUCTION

Spin-on dielectric (SOD) materials have generated much interest as alternatives to chemical vapor deposition (CVD) and high density plasma (HDP) deposited materials for isolation purposes in future semiconductor devices.[1–3] SOD can be tailored to specific applications in semiconductor processing, including shallow trench isolation (STI), premetal dielectric (PMD), and interlayer/metal dielectric,[4,5] with each application requiring enhancement of certain properties of the material. For STI, the foremost requirement for candidate SOD material is uniform, void-free gap filling of STI trenches. Up to now, expensive HDP-CVD and subatmospheric CVD technologies have been widely used for STI purposes.[6,7] These technologies already have difficulty in gap filling[8] and are becoming increasingly complex and costly to continue meeting the requirements of industry. With a move toward more density in semiconductor devices, smaller and higher aspect ratio trenches make void-free gap filling incrementally challenging. STI trench aspect ratio in memory devices is expected to be well beyond 10, even approaching 20, in the next 10 years.[9] With such high aspect ratios, continued use of conventional HDP-CVD technologies alone would be unfeasible by virtue of prohibitive costs and/or inadequate gap filling. SOD materials are poised to meet and even exceed these increasingly stringent requirements. Therefore, the 2007 International Technology Roadmap for Semiconductors (ITRS) terms SOD as "mandatory to fill very high aspect ratio trenches."[9]

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During the development process of SOD, a low cost test bed of large area high aspect ratio nanotrenches, with widths corresponding to poly half-pitch dimensions of future memory devices, is highly desirable. However, fabrication of ultrahigh aspect ratio nanotrenches over large areas is expensive and time consuming, as patterning must often be done by state-of-the-art photolithography tools or electron beam lithography. The cost and associated challenges are further exacerbated by the amount of samples required during the development process. In this work, we first demonstrate fabrication of ultrahigh aspect ratio nanotrenches (AR of >30, trench width ~ 22 nm) as test bed STI structures for the 22 nm semiconductor node using nanoimprint lithography followed by a dimension reduction technique. Transmission electron microscopy (TEM) is used to evaluate gap filling property of proprietary new polysilazane based SOD (Dongjin Semichem) after curing in oxygen. We show that this type of SOD material is able to fill sub-25 nm wide ultradeep trenches ($AR > 30$) without voids. Fourier transform infrared (FTIR) spectroscopy analysis is used to characterize the curing properties of the SOD, showing that the material can be cured in oxygen at temperatures over 600 °C. This work indicates that SOD has strong potential for meeting STI requirements for the 22 nm node and beyond.

II. NANOTRENCH FABRICATION

Ultrahigh aspect ratio nanotrenches are fabricated by nanoimprint lithography and plasma etching using a dimension reduction technique, which is discussed in more detail

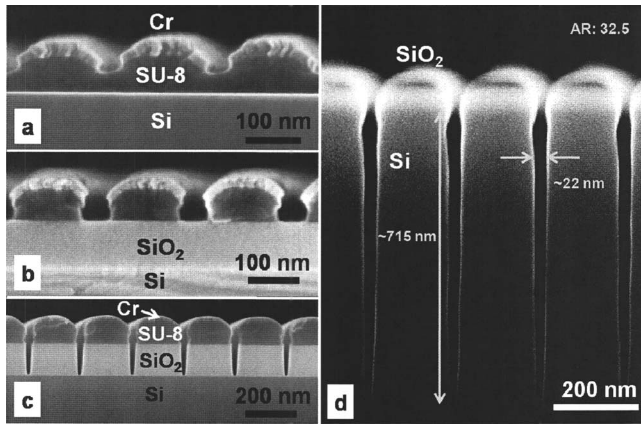

FIG. 1. Cross sectional SEM images of (a) a typical sloped SU-8 profile selectively coated with Cr after the dimension reduction process, (b) a typical profile with the exposed SU-8 residue removed, (c) patterns transferred to the oxide layer, and (d) patterns transferred to Si, yielding ultrahigh aspect ratio nano-trenches.

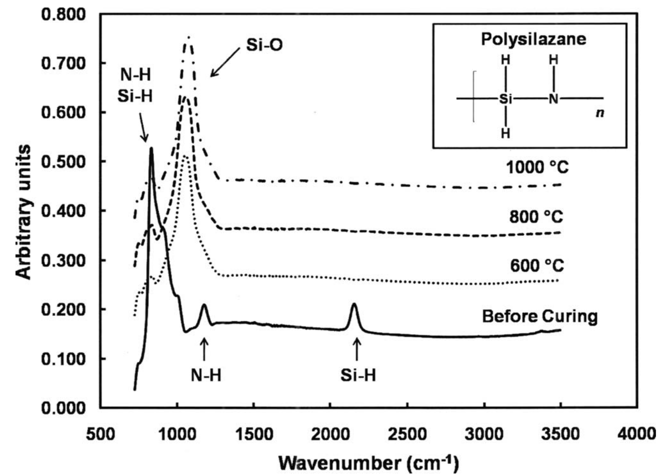

FIG. 2. FTIR data comparing the chemical makeup of polysilazane films before and after curing for 1 h at 400, 600, and 1000 °C. The inset shows the chemical structure of polysilazane SOD.

elsewhere.[10] A layer of SU-8 was spin coated onto an oxidized silicon wafer with 150 nm top oxide thickness, followed by nanoimprint with a Si mold containing 100 nm line and space patterns over a large area (~ 6 cm^2). The mold is treated with perfluorodecyltrichlorosilane (FDTS) to prevent adhesion of SU-8 to the mold during demolding. This larger nanoimprinted grating pattern underwent a dimension reduction process involving shadowed chrome (Cr) evaporation, reducing the effective pattern dimensions in SU-8, before transfer to the underlying layers [Figs. 1(a) and 1(b)]. Figure 1(a) contains a cross section of patterns on Si to show the uniformity of the dimension reduction process with shadowed Cr evaporation. Samples used in this study are fabricated on oxidized silicon wafers [Fig. 1(b)]. Next, an oxygen plasma etch, followed by a high power plasma etch in a mixture of C_4F_8, CHF_3, and Ar, transferred the patterns down to the oxide layer [Fig. 1(c)]. The conditions for the oxide etch have been optimized to yield a vertical profile with minimal slope, as the quality of the oxide mask determines the dimensions and profile of the final Si nanotrench. Next, the remaining Cr and SU-8 were removed using CR-9S Cr wet etchant and piranha solutions. The pattern was transferred into Si with a chlorine (Cl_2) plasma etch (300 W inductively coupled plasma power, 100 W bias power, 5 mTorr, 60 °C chuck temperature), as shown in Fig. 1(d). The average Si etch rate at these conditions is ~ 8 nm/s. However, the actual etch rate is much faster toward the beginning of the etch and slows down as the etch progresses deeper, as the removal of etch by-products from the deep nanotrenches becomes slower. Therefore, the sidewalls of the nanotrenches begin to slope as the etch progresses deeper, resulting in a trench bottom (~ 10 nm) that is about half the size of the trench opening (~ 22 nm). It is worth noting that there is ~ 25 nm of oxide mask remaining after the Si etch, indicating that the selectivity of Si etch rate to SiO_2 etch rate is quite high (~ 6). With the given high selectivity, the nanotrenches can be etched even deeper. However, as can be seen in Fig. 1(d), the trench profile slope increases with deeper etching. Hence, if the etching time was increased, the etch rate in the vertical direction would decrease to a point at which no more etching would occur; at this point, nonuniform sputtering and redeposition of by-products combined with a finite horizontal etch rate would lead to widening of the trenches in a nonuniform manner. In order to preserve uniformity in trench shape and depth, the nanotrenches were etched to a depth of ~ 715 nm. At this depth, the aspect ratio is ~ 32, which is well beyond the STI aspect ratio requirements for future memory devices. After nanotrench fabrication, the remaining oxide mask was removed by wet etching in buffered oxide etch solution. The sample underwent an RCA cleaning process to remove any organic and inorganic contaminants.

III. SOD GAP FILLING

The ultrahigh aspect ratio nanotrenches serve as a test bed for analysis of SOD gap filling characteristics. The polysilazane based SOD (inset of Fig. 2) is a solution processed thermally curable material, in dibutly ether solvent, with viscosity of ~ 1.7 cst and an average molecular weight of $\sim 10\,000$ (Dongjin Semichem). In general, depending on the viscosity of solution, the spin coating conditions can have an effect on final filling profile. However, polysilazane solution has low viscosity and does not seem to require strict optimization of spin conditions. The solution was spin coated into the nanotrenches at a speed of 1500 rpm for 30 s in an enclosed spin coater with an ambient atmosphere. The sample was heated on a hot plate at 150 °C for 3 min to remove residual solvent. The sample was thermally cured at high temperature to facilitate conversion of the SOD material inside the nanotrenches to oxide, as is required in STI application. Analysis of filling must take place after this thermal curing step, as the thermal curing process can potentially change the filling quality by introducing voids.

During the thermal curing process, the material is engineered to be converted to a dense Si–O network with prop-

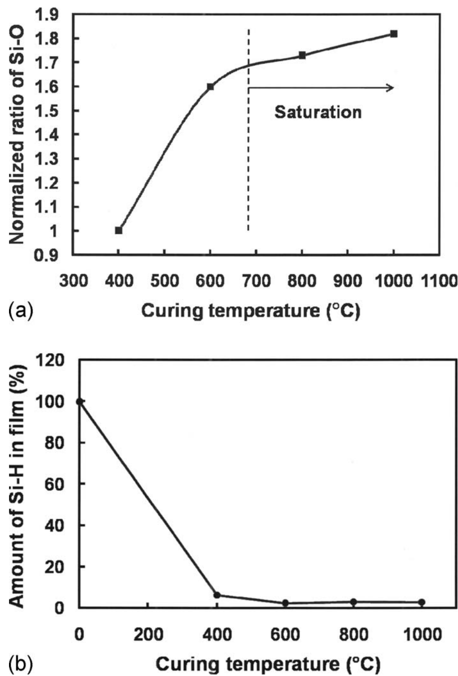

FIG. 3. (a) Ratio of the area of the Si–O peak as a function of curing temperature, normalized with respect to 400 °C. (b) The amount of Si–H in the film as a function of curing temperature. Curing time is 1 h for all samples.

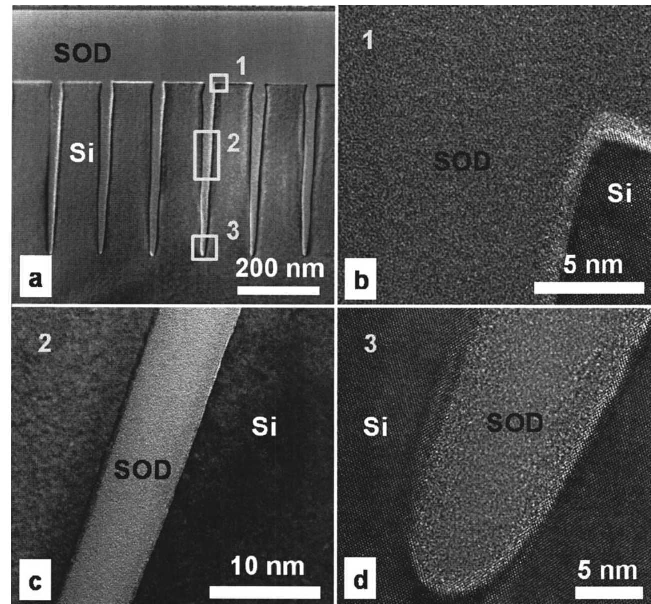

FIG. 4. Cross sectional TEM images showing (a) an overview of filling across multiple nanotrenches, (b) filling near the top of the nanotrench, (c) filling in the middle of the nanotrench, and (d) filling at the bottom of the nanotrench.

erties similar to thermal oxide. As the SOD is cured, the nitrogen and hydrogen in the SOD leave the material and are replaced by oxygen to form Si–O bonds. As such, curing is usually done in a high temperature, oxygen rich environment, much like an oxidation furnace. To determine optimal curing conditions, several samples with SOD spin coated directly onto the unpatterned Si wafers were cured for 1 h at different temperatures in an oxidation furnace in the presence of continuously flowing O_2 gas. FTIR analysis was done to determine the chemical makeup of the films cured at different temperatures, with respect to that of the uncured film. As shown by FTIR data in Fig. 2, the chemical structure of the film after curing is completely changed from the uncured state; after curing, the Si–H, Si–N, and N–H are absent from the film, replaced instead by a large concentration of Si–O. The results seem to indicate that the Si–H and Si–N in the film are removed quickly and Si–O forms without much dependence on temperature. However, the Si–O peak intensity increases with temperature. Figure 3(a) shows the ratio of the area of the Si–O peak as a function of curing temperature, normalized with respect to 400 °C, indicating higher density of Si–O bonds forming with increasing temperature. The amount of Si–O changes significantly with increasing temperature, up to about 600–800 °C, after which the change is relatively small. Figure 3(b) shows the amount of Si–H in the film as a function of curing temperature. The Si–H bond density drops quickly and reaches negligible levels after 400 °C. These results show that a curing temperature greater than 600 °C would be adequate. Therefore, to ensure complete curing, SOD in nanotrenches was cured in a dry O_2 environment at 800 °C for 1 h in an oxidation furnace. Next, the sample was prepared for cross sectional TEM imaging by focused ion beam. As shown in Fig. 4, cross sectional TEM analysis finds no voids in cured SOD material inside the nanotrenches. The filling is excellent and uniform in multiple adjacent nanotrenches, as shown in Fig. 4(a). The topside of the SOD, on the surface of the sample, is exceptionally planar, which is one of the many benefits of SOD. For complete analysis, the full length of the nanotrench was imaged. The filling is flawless throughout the entirety of the trench, even down to the bottom of the trench with a width of 5–10 nm, as seen in Fig. 4(d). As evidenced by this analysis, not only is the initial filling void-free, but, remarkably, the thermal curing process does not introduce any voids. Such stability after thermal curing is required in STI application. Exceptional filling and stability in ultrahigh aspect ratio nanotrenches, which are challenging for the most complex and expensive HDP-CVD methods, seem to be inherent to polysilazane SOD material.

IV. CONCLUSION

In this work, we demonstrate fabrication of ultrahigh aspect ratio nanotrenches over a large area by using nanoimprint lithography combined with a dimension reduction technique. We have used these nanotrenches to demonstrate the viability of polysilazane SOD for STI application at the 22 nm node and beyond. This material meets and exceeds the requirements for high aspect ratio gap filling through the end-of-roadmap for future semiconductor memory devices. To the best of our knowledge, we have demonstrated the highest aspect ratio gap filling of SOD material in Si nanotrenches.

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