

EE6304: Computer Architecture
Mid-Term Exam, October 21, 2009
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Name:	Score: / 100
ID:	

*Note: Exam is CLOSED-BOOK EXAM.
(total number of points is 100, each question is marked with no. of points)*

1. (10p) Associate one machine with each statement:

- (a) early version had no operating system **PDP-8**
- (b) first family of computers **IBM 360**
- (c) first computer to have index register **IBM 704**
- (d) introduced 8-bit byte **IBM Stretch**
- (e) introduced I/O architecture **IBM 702**
- (f) included multiple functional units **IBM 360/91**
- (g) introduced I/O channels **IBM 709**
- (h) does not have PC relative addressing **IBM 360**
- (i) first electronic general purpose computer **ENIAC**
- (j) first proposed stored program computer **EDVAC**
- (k) Harvard architecture **MARK - III**

2. (10p) Circle the items that are part of the definition of **computer architecture**, cross the ones that are not a part of **computer architecture** definition:

- (a) instruction set
- (b) clock speed **x**
- (c) addressing modes
- (d) register file
- (e) pipeline organization **x**
- (f) number of floating-point registers
- (g) number and type of floating-point execution units **x**
- (h) floating-point formats
- (i) memory size **x**

3. (20p) Assume the following instruction statistic:

R-to-R Machine:

L/S40% 2-cycles

Branch ...15% taken, 2-cycles
...5% not-taken, 1-cycle

ALU40%, 1-cycle

(a) What is the average CPI ? (5p)

$$0.4(2) + 0.15(2) + 0.05(1) + 0.4(1) = 1.55$$

(b) If Memory-to-Register architecture will change the distribution to:

M-to-R Machine:

L/S20% 2-cycles

Branch ...15% taken, 2-cycles
...5% not-taken, 1-cycle

ALU60%, 2-cycles

How would CPI be changed? (5p)

$$0.4(2) + 0.15(2) + 0.05(1) + 0.4(2) = 1.95$$

Would this change result in performance improvement? no

(c) (5p) assuming that only L/S and ALU operations percentages will change in changing from R-R to R-M architecture (with given CPI numbers), what is the distribution that will make them equal?

(assume that decrease in L/S for x% results in equal x% increase of ALU operations) (10p)

80% LS

0% ALU

Using R-R percentages

(d) (5p) What is the CPI in the R-R machine if caches are added with the following parameters:

- Data Cache 4% miss ratio, Instruction Cache 5% miss ratio: 1-cycle access and 10-cycle miss penalty? (10p)

$$\begin{aligned} & (\text{DataMem} + \text{ALU} + \text{Branch}) * (\text{InstAccess}) \\ & (0.4(0.04(10) + 0.96(1)) + 0.4 + 0.15(2) + 0.05(1)) * (0.95(1) + 0.05(10)) = 1.294 * 1.45 = \\ & 1.8763 \end{aligned}$$

4. (10p) List:

(a) (5) three problems (inaccuracies) associated with using MIPS as a measure of performance for comparison of different machine performance.

Does not account for instruction complexity
Does not account for program
Compiler dependent

(b) (5) three problems (inaccuracies) associated with using MFLOPS as a measure.

Similar to above

5. (5p) Which machine M-to-M or R-to-R has lower number of total memory references (instructions+data)? Explain why?

R-R, every intermediate instruction has to access data memory for an M-M machine, while true that load and store instructions are not needed in an M-M machine, Load and Store can account for a very small percentage of overall instructions in many applications.

6. (5p) The frequency of branches on IBM S/360 is found to be about 16% versus 23% on the DEC VAX-11. What does this tell you about the instruction set architecture? Explain.

DEC VAX-11 has a complex instruction ISA, thus fewer instructions are used between branches that accomplish the same function.

7 (10p) IBM S/370 does not have indirect addressing. Assume that the address of an operand is stored in main memory. How would you access the operand?
(show the sequence of operations / instructions)

Addr = memory location where operand address is stored

Movi R1, Addr

; R1 now contains the memory address where the address for the operand is stored

LW R2, (R1); operand now in R2

8. (10p) List the 9 features that characterize RISC architecture?

- Load/Store architecture
- Carefully selected set of instructions
- Fixed format of instructions
- Simple addressing modes
- Separate instruction and data cache
- Delayed branch
- Optimizing compiler
- Goal of a CPI of 1.0
- Pipelining support

9 (5p) RISC architecture rely to a great extent on the availability of current information in registers. Can the number of registers be arbitrarily increased? Explain.

No, increasing the number of registers also increases the cost for accessing the registers.

10. (15p) To add support to register-memory ALU operations, all memory addressing will be restricted to addresses being simply a value held in a register and so no offset. For example, the register-memory instruction ADD R4, R5, (R1) means add the contents of registers R5 to the contents of memory location with address pointed by value in register R1, and write the sum to register R4. Register-register ALU operations remain unchanged. To facilitate this, the MIPS five-stage pipeline can be redesigned with stages as IF, ID, MEM, EX, and WB. Now, for such a pipeline, consider the following instruction code sequence:

```

Loop:  sw    R5, (R4)
       add  R3, R5, (R4)
       or   R7, R3, R5
       sub  R3, R7, R7
       beqz R3, Loop
    
```

- (a) (5p) Identify all the data (RAW) and name (WAW, WAR) dependencies among registers and memory references
- RAW from (1) -> (2) in the memory reference of R4 (write to location (R4) then read location (R4))
 - RAW from (2) -> (3) register R3
 - RAW from (3) -> (4) register R7
 - WAR from (3) -> (4) register R3
 - WAW from (2) -> (4) register R3
 - RAW from (4) -> (5) register R3
- (b) (5p) For the given modified MIPS 5-stage pipeline without any forwarding or bypassing hardware, show the pipeline timing of this instruction sequence (use the given table below). Assume the availability of forwarding within the register file, when a register is read and written in the same clock cycle. Assume a zero branch test is done in the decode stage, and all memory references are a cache hit.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Sw	F	D	M	X	WB														
Add		F	D	M	X	WB													
Or			F	S	S	D	M	X	WB										
Sub						F	S	S	D	M	X	WB							
Beqz									F	S	S	D	M	X	WB				
Sw												F	D	M	X	WB			

- (c) (5p) For the given modified MIPS 5-stage pipeline, now with full forwarding hardware, show the pipeline timing of this instruction sequence (use the given table below). Take the rest of all assumptions to be the same as in (b).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Sw	F	D	M	X	WB														
Add		F	D	M	X	WB													
Or			F	D	M	X	WB												
Sub				F	D	M	X	WB											
Beqz					F	S	S	D	M	X	WB								
Sw									F	D	M	X	WB						