

Design of a Lock-in Amplifier For Terahertz Detector And Imager Arrays on Monolithic CMOS

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Abstract

This work describes the design and integration of a lock-in amplifier with a terahertz detector array. Research in the terahertz region, which lies between the microwave and infrared portion of the electromagnetic spectrum, has been on the rise due to its potential applications as a biologically-safe replacement for X-Ray imaging and other non-invasive applications such as spectroscopy. Cryogen-cooled bolometers and devices based on compound semiconductors such as Gallium-Arsenide are currently the industry-standard for terahertz detection. However, these devices have major drawbacks such as the use of cryogenics, high cost, and inability to realize a large array. CMOS-based (complementary metal oxide semiconductor) detectors have none of those drawbacks, however the detector noise exceeds that of the industry-standard. This project combines the advantages of both the industry-standard and CMOS-based detectors into one monolithic CMOS chip. A specially designed lock-in amplifier is integrated with the CMOS-based detectors to improve the signal-to-noise ratio. The chip was successfully designed and simulation confirms that it has the ability to attenuate unwanted frequencies while providing gain of 70dB on the desired detected signal. The chip has recently been fabricated in United Microelectronics Corporation's (UMC) 130nm logic/mixed-mode 1.2V RF CMOS process and is expected to be ready for testing by mid-December.

1 Introduction

1.1 Background

Research within the terahertz (THz) frequency range (300GHz – 3THz) of the electromagnetic spectrum has been becoming increasingly active due to its potential for use as a medically-safe alternative to X-Ray. Other THz applications include: concealed weapon detection, early cancer detection, spectroscopy, short range radar, secured high-speed data communications, aviation assistance, remote explosives detection, remote substance identification, and non-invasive measurements [1]-[5]. Unlike the frequency range of X-Rays (10^{18} Hz), the terahertz frequency range is between the microwave and infrared range. The location of the terahertz band on the electromagnetic spectrum is generally safer for biological tissue because it is within the non-ionizing section of the electromagnetic spectrum. Some future applications that require specific characteristics of X-Rays, such as its ability to propagate through non-metallic objects, may instead prefer to use terahertz because of the relatively lower frequency. Furthermore, it is accessible by solid state electronics, lower power consumption, can operate at room temperature, small size, and easy to manufacture [6]-[8].

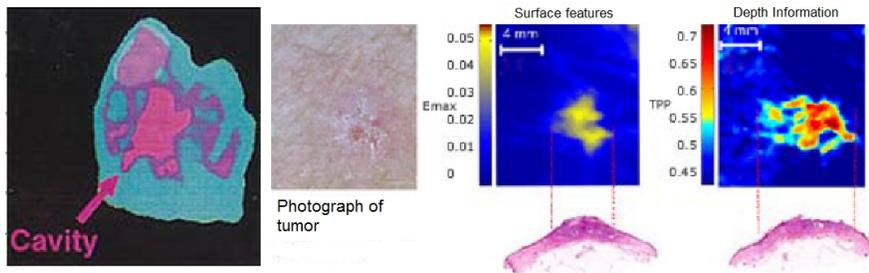


Illustration 1: Spectroscopy example applications using terahertz. (Left) Early detection of tooth cavity. (Right three) Terahertz spectral images for early detection of a deadly form of skin cancer. All measuring procedures are non-invasive.

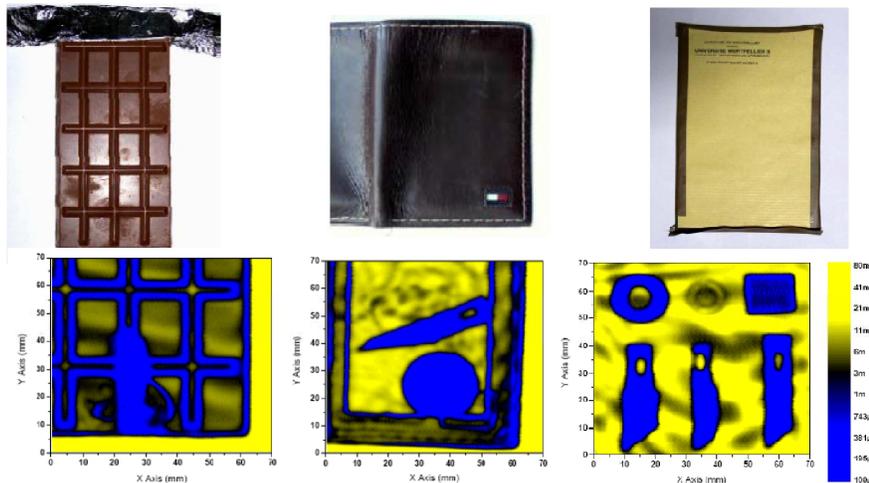


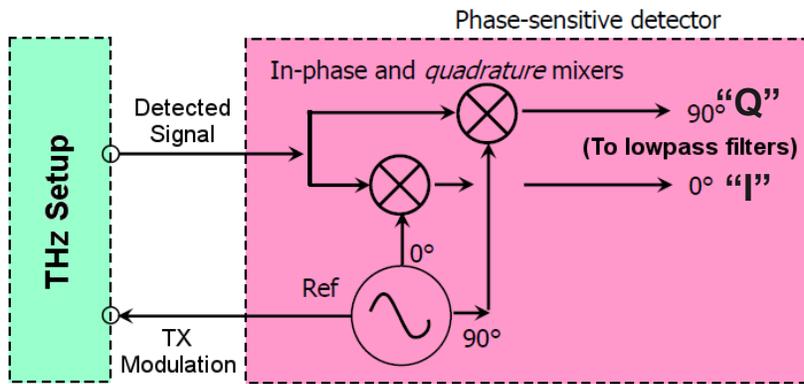
Illustration 2: Terahertz imaging example applications using terahertz. Shown are three images (bottom row) obtained by concealing metallic objects in a chocolate bar, wallet, and an envelope.

A terahertz detector is one of the most fundamental building blocks in terahertz systems, enabling the system to “tap” into and assess the terahertz spectrum. Devices such as cryogenic-cooled bolometers and detectors fabricated on non-standard semiconductor alloys (e.g. Gallium-Arsenide) are usually employed in modern-day laboratory and industrial settings for terahertz detection. These devices are perhaps the most accurate and most reliable methods of terahertz detection. Typically these devices are large, high mass, expensive, and not easy to manufacture^[8]. The majority of the drawbacks originate from the cryogenic cooling system which is necessary to increase the signal-to-noise ratio (SNR) and sensitivity of the detector. Noise reduction is achieved by reducing noise contributions from background “cosmic” terahertz radiation and blackbody radiation^{[10][11]}. These traits stand out as undesirable in most situations when compared to a monolithic terahertz detector that utilizes standard CMOS (complementary metal-oxide semiconductor) fabrication technology.

Terahertz detectors that operate at 280 GHz, 540 GHz, and 860 GHz used as imaging arrays were recently fabricated using Schottky barrier diodes (SBD) on 130nm CMOS technology without any process modifications^{[6][7]}. The imaging functionalities of these chips were tested in a setup that required no mirrors or lenses which would otherwise add size and cost to the end application^[7]. The SNR and sensitivity of these chips are inferior to that of cryogenic-cooled and non-standard semiconductor alloy detectors. This is because unwanted noise from background radiation, including blackbody radiation, and flicker ($1/f$) noise is significantly higher due to room temperature operation and the nature of CMOS^[9]. Using CMOS chip-based terahertz detectors at room temperature is problematic because the detector-related noise is directly proportional with temperature and inversely proportional to the sampling duration. Setups that use detectors that operate in room temperature often incorporate a lock-in amplifier to bypass this problem. A lock-in amplifier is a scientific instrument resembling a homodyne direct conversion receiver. The homodyne architecture effectively acts as a high-Q bandpass filter to distinguish between the desired signal from the background noise^[12]. Most lock-in amplifiers used in laboratory settings, including the setups used to test the 130nm CMOS detectors, are often in the form of a general purpose, heavy, rack-mounted unit that operates on 120VAC standard electricity. The use of such scientific instrumentation outweigh the advantages of using a CMOS chip-based terahertz detector^{[4][7]}.

1.2 Lock-in Amplifier

There are two types of lock-in amplifiers (LIA): dual phase and single phase. The dual phase type is used in precision instrumentation due to its ability to distinguish amplitude from phase. A dual-phase lock-in amplifier resembles an I/Q homodyne radio receiver followed by a



$$V_{DC(I)} = V_{RMS} \sin(\Theta_{IN})$$

$$V_{DC(Q)} = V_{RMS} \cos(\Theta_{IN})$$

Equation 1

$$R = \sqrt{I_{OUT(DC)}^2 + Q_{OUT(DC)}^2}$$

Equation 2

$$\Theta_{OUT} =$$

$$I_{OUT(DC)} > 0 : -\arctan\left(\frac{Q_{OUT(DC)}}{I_{OUT(DC)}}\right)$$

$$I_{OUT(DC)} < 0 : 180 - \arctan\left(\frac{Q_{OUT(DC)}}{I_{OUT(DC)}}\right)$$

Equation 3

Illustration 3: Block diagram of a dual-phase lock-in amplifier (lowpass filters omitted) for terahertz applications. The modulation frequency for this case will be a 10MHz square wave. The detected signal amplitude is expected to be less than 1mVp-p with a low SNR. Image from [16].

Total noise in 10 Hz bandwidth

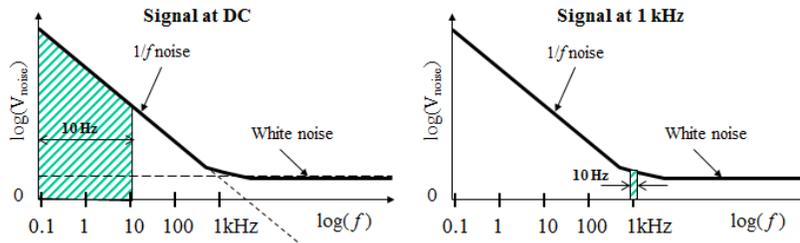


Illustration 4: Spectral representation of flicker noise. The basic purpose of the lock-in amplifier is to shift the signal towards a known higher frequency. Notice that the noise is higher at lower frequencies than at higher frequencies with the same bandwidth due to flicker noise..

lowpass filter. There are two main ideas behind the operation of the lock-in amplifier. First, the modulation signal source, represented by “Ref” in *Illustration 3*, modulates the desired signal to a known frequency of f_{REF} that is away from flicker noise. The effects on the SNR by the modulation can be graphically represented by *Illustration 4*. Second, the mixing and lowpass actions combined acts as an effective bandpass filter whose passband region is expressed as $f_{REF} \pm f_{LOWPASS}$ where $f_{LOWPASS}$ is the bandwidth of the lowpass filter [12]-[15]. For optimal performance, $f_{LOWPASS}$ is generally chosen to be $f_{LOWPASS} \ll f_{REF}$. Assuming two identical lowpass filters exist at the outputs of “I” (inphase) and “Q” (quadrature), the DC component of I and Q can be calculated using *equation 1* based on V_{IN} and Θ , the input amplitude and phase at frequency f_{REF} relative to the reference source (“Ref” in *Illustration 3*). *Equation 2* describes the lock-in derived amplitude and *equation 3* describes the phase of the signal relative to the reference signal. As shown in *Illustration 3*, the terahertz signal will be modulated using the “Ref” signal source similar to amplitude modulation because, currently, it is easier and more cost-effective to use terahertz as a carrier signal rather than the desired signal.

1.3 End Product

This engineering project stems from the recently developed 130nm CMOS 860 GHz SBD detectors. In the end, a monolithic “system-on-chip” terahertz detector array for imaging applications that requires minimal external components necessary for basic functionality is realized by incorporating an on-chip lock-in amplifier with the detectors on standard 130nm CMOS technology without any process modifications, also graphically shown in *Illustration 5*. Because this new chip will combine a lock-in amplifier with the CMOS-based detectors, the advantages that were both mutually exclusive to bolometer/cryogenic devices and CMOS terahertz detectors can now be realized on one monolithic CMOS-based system-on-chip terahertz detector. Currently, there are no published works of a monolithic CMOS THz detector with a signal processor (lock-in amplifier). This lock-in amplifier also outperforms, currently according to simulation, other similar works in various parameters such as chip area, maximum operating frequency, and power consumption ^{[13][14]}.

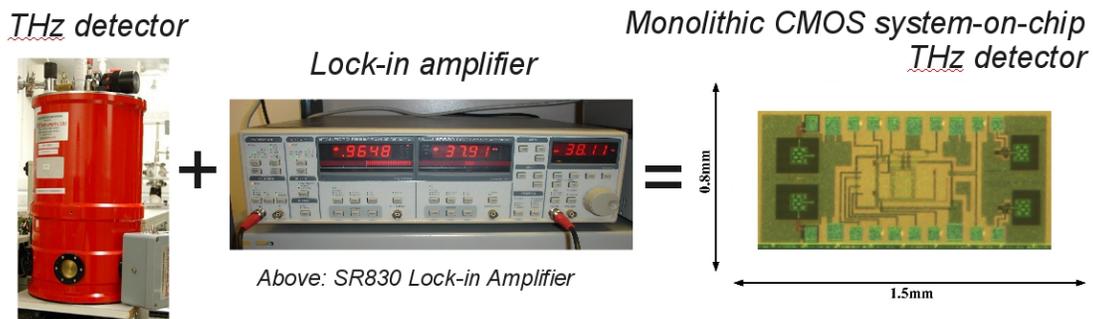


Illustration 5: The goal, components, and end product of this project, in simple terms.

2 Problem

An ordinary dual-phase lock-in amplifier cannot be directly designed into CMOS due to two main problems, where the first problem is the cause of the second problem.

The first problem is that the typical lock-in amplifier must be AC-coupled or else the circuit would not function properly if it is intentionally given DC voltage at the input. This is particularly important because DC bias is required for the detector diode's operation. The addition of an offset voltage in a DC-coupled lock-in amplifier can be expressed by adding the term V_{OFFSET} to both equations in *equation 1*. Note that a third variable has been introduced, making it a two-statement system of equations with three variables, and thus the term V_{OFFSET} cannot be distinguished from the actual desired amplitude itself. The output would now be a linear function of the offset voltage, which usually is unknown and unpredictable, and a function of the actual input amplitude.

Secondly, AC-coupling (DC-blocking) capacitors cannot be used in this circuit. Normally,

a capacitor is used in series to block DC voltages. This cannot be satisfied neither on-chip nor off-chip due to practicality issues. The capacitance value that is suitable for the frequency of f_{REF} would be too large to be practically fabricated on-chip. Furthermore, if the capacitor is located off-chip, then excessive chip area must be occupied to allow for a minimum of two bondwire pads per capacitor. Placing the capacitors off-chip is practical for small imaging arrays, however, it would rapidly become impractical as the number of imaging pixels (detectors) increase. Furthermore, although sharing one lock-in amplifier and a off-chip capacitor is possible for an array of detectors, the bandwidth allocation per detector may become extremely inefficient due to the required bandwidth of the lowpass filter. In this case, it is best to assume the lock-in amplifier is being designed for a large imaging array for the sake of scalability, continuity of the design, and real-world applications.

As a result, the nature of the design itself must be immune to DC offsets by itself.

3 Solution

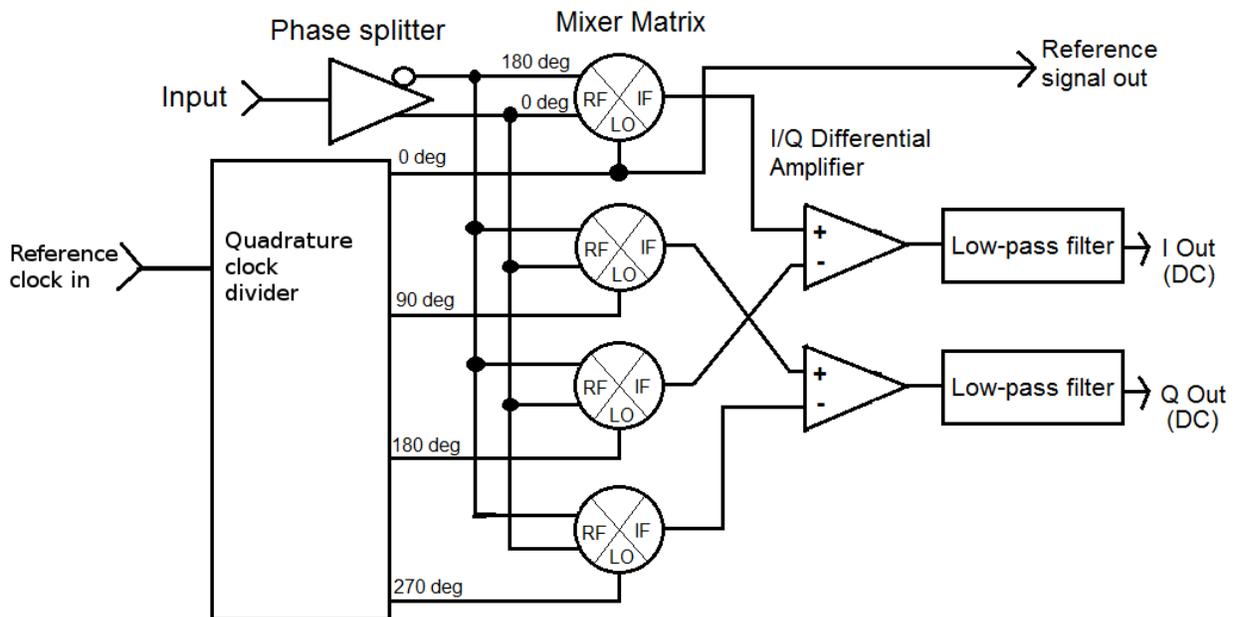


Illustration 6: block diagram of the dual-phase differential lock-in amplifier

$V_{IF(0)} = V_{RMS} \times \cos(\Theta_{IN})$	$V_{IF(90)} = V_{RMS} \times \sin(\Theta_{IN})$	$V_{IF(180)} = -V_{RMS} \times \cos(\Theta_{IN})$	$V_{IF(270)} = -V_{RMS} \times \sin(\Theta_{IN})$
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Equation 4

$V_{DC(I)} = V_{IF(0)} - V_{IF(180)}$

Equation 5

$V_{DC(Q)} = V_{IF(90)} - V_{IF(270)}$
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Equation 6

For this project, a new type of lock-in amplifier, named the “dual-phase differential” lock-in amplifier, is designed. The block diagram of this design is shown in *illustration 6*. This type of lock-in amplifier has differential I and Q channels to cancel out DC offset errors originating from

external conditions. The function and purpose of the lock-in amplifier is unchanged because the desired DC signal that is the result of direct conversion is preserved.

Equation 4 describes the DC output of each mixer as a function of the desired input signal's amplitude and phase, where ϕ_{xx} indicates the mixer's LO phase in $V_{IF(xx)}$.

Equation 5 and 6 applies equation 1 and 4 to the dual-phase differential architecture. Two types of offset voltages, common-mode and unbalanced offset, exist within differential circuits. The common-mode voltage can be thought of as the instantaneous average of the DC potential between the inverting and non-inverting signals in a differential circuit. Common-mode offset is the difference between the differential signal's actual common-mode voltage compared to the ideal common-mode voltage. On the other hand, unbalanced offset is the difference between the non-inverting signal's DC voltage to the common-mode voltage and the inverting signal's DC voltage to the common-mode voltage. The effect of both types of offset voltages can be thought of as common-mode offset voltage because both types yield a shift in the common-mode voltage of the differential signal. In a standard lock-in architecture, this common-mode offset voltage would propagate directly to the output because it is terminated as a single-ended signal and thus causes the circuit to function improperly and give erroneous results. In a dual-phase differential architecture, this common-mode offset propagates through all four mixers and the offset is nullified at the I/Q differential amplifiers.

3.1 Proof of Concept

$V_{IN}=200mVp-p; f_{ref}=f_{in}=100kHz; \Theta_{IN}=0; f_{LPF(-3dB)}=1kHz, LPF\ Order = 8$				
Offset voltage (mV)	Unbalanced Offset (mV)		Common-mode Offset (mV)	
	R	Error Ratio (dB)	R	Error Ratio (dB)
0 (IDEAL)	108.76	0.000	108.76	0.000
1	108.77	0.001	108.76	0.000
2	108.79	0.002	108.76	0.000
3	108.80	0.004	108.76	0.000
4	108.82	0.005	108.76	0.000
5	108.83	0.006	108.76	0.000
6	108.85	0.007	108.76	0.000
7	108.86	0.009	108.76	0.000
8	108.88	0.010	108.76	0.000
9	108.89	0.011	108.76	0.000
10	108.91	0.012	108.76	0.000

Table 1: Preliminary offset voltage versus output behavioral simulation of the dual-phase differential lock-in amplifier architecture

A preliminary SPICE simulation was done using behavioral models to confirm this theory. The signal sources were modeled as ideal voltage sources, mixers as ideal voltage-controlled-switches, operational amplifiers as voltage-dependent-voltage-sources, and the lowpass filters are described using the Laplace transform function. Other performance measures that are dependent on "real-world" design are not examined because this behavioral

simulation is too idealized to yield accurate benchmarks of exact performance. Furthermore, the SPICE simulator used for this proof of concept does not support periodic steady state analysis (PSS). Thus, using this to predict frequency response would require non-standard simulation techniques that can yield questionable results.

The theory is indeed confirmed in *Table 1*. A range of reasonable offset voltages for modern-day 130nm CMOS process is injected into the input signal in both forms, unbalanced and common-mode, and the value “R” is calculated based on the lock-in amplifier’s outputs using *equation 2*. The simulation run with an offset voltage of 0mV is used as a reference for comparison because the effective value of V_{OFFSET} is zero. The error ratio of each simulation run compared to the ideal simulation run (offset voltage of 0mV) is also calculated and expressed in the form of a log (decibel) ratio. The simulations show that any DC offset introduced to the input has a negligible effect on the output accuracy, when compared to the standard lock-in amplifier architecture where the output is directly linear with the input offset voltage. The simulations also show that the new lock-in architecture has near ideal immunity to common-mode offset voltage. Immunity to unbalanced offset voltages yields approximately 0.012dB error per 10mV of offset. This rate of error can be considered negligible because 10mV is about the nominal offset voltage in CMOS devices with careful matching in the layout of the chip. It can also be theorized that this theory may hold true for the entire operating range of the lock-in amplifier because switching mixers, in general, have high linearity.

4 Design

The abstract block diagram in *Illustration 6* was then adapted for fabrication in United Microelectronics Corporation’s (UMC) 130nm logic/mixed-mode 1.2V RF CMOS process. The major sub-circuits of the chip include: four 860 GHz antennas with Schottky detector diodes, a fully-differential low noise amplifier (phase splitter), four passive switching mixers (mixer matrix), two operational amplifiers (I/Q differential amplifiers), and a clock divider. All chip designs and simulations were done in Cadence Virtuoso and Spectre software, respectively. The chip is comprised of primarily N-type enhancement and P-type enhancement metal-oxide field effect transistors (NMOS and PMOS, respectively) and passive silicon components. All body connections for NMOS and PMOS transistors are tied to GND and VDD terminals, respectively, unless otherwise drawn on the schematic. Design goals for the lock-in amplifier include operating frequency up to 10MHz and an on-chip lowpass filter of 100kHz.

4.1 860 GHz Detector

This chip would obviously not be considered a “terahertz detector” if the circuitry to

detect the terahertz signal is not present. The design of the detectors are provided by a graduate student that belongs in the same lab group, thus this circuit block will not be described in detail. The design of the detectors were provided and is not the original work of the designer for two main reasons. First, the designer has no prior experience whatsoever in the discipline of terahertz circuitry on CMOS. This specific discipline is still relatively very young and almost exclusively limited to graduate students and higher. Secondly, the main focus of this project is the design of the lock-in amplifier that is applied to improving terahertz detection technology. As a result, the detector design was provided to maintain consistency of the research. Otherwise, should the designer have originally designed the detectors and not use what is provided, this would be a confounding variable to the effectiveness and functionality of the lock-in amplifier.

The design of the detector is relatively simple and similar to that of a basic AM crystal radio receiver. An on-chip patch antenna is used to receive the 860 GHz signal which is then fed into an impedance matching network and finally into the Schottky barrier diode. The purpose of the diode acts as a self-mixer and converts the amplitude of the 860 GHz signal down to baseband. In essence, it acts as the equivalent to a diode envelope detector used in simple AM radios. The output of the diode is then routed to other parts of the chip where the detected signal is used. This is also the point where DC bias is introduced into the diode. In the layout, a parasitic lowpass filter is formed between the diode and the output and thus prevents any high-frequency (i.e. terahertz) signals from going anywhere else but the detector diode.

4.2 Fully-Differential Low-Noise Amplifier

Illustration 7 shows the complete schematic of the fully-differential low-noise amplifier (LNA). The LNA's main purpose is to lower the impedance of the detector's signal while isolating the noise from the mixer's inputs from the detector's signal. A low-noise front-end gain stage is needed to interface with the detectors because previous experiments with the 860 GHz SBD detectors show that the detectors can only tolerate up to $5nV/\sqrt{Hz}$ of input-referred noise from the succeeding stage for acceptable performance. The design of the fully-differential low-noise amplifier consists of a folded-cascode first stage followed by an NMOS buffer stage. The PMOS devices offer lower $1/f$ noise compared to the NMOS devices. The PMOS transistors were optimally sized to reduce $1/f$ noise. The body connections of the PMOS transistors are tied to the source terminals instead of VDD to reduce parasitic capacitance and to optimize the frequency performance for the large PMOS transistors. $C1$ and $C2$ are compensation capacitors of 1.25pF each. These capacitors add an extra pole in the system transfer function and help shift the roll-off frequency in the open-loop AC response to ensure phase margin and stability. $R1$ and $R2$ act as a simple common-mode feedback circuit to bias the current mirror

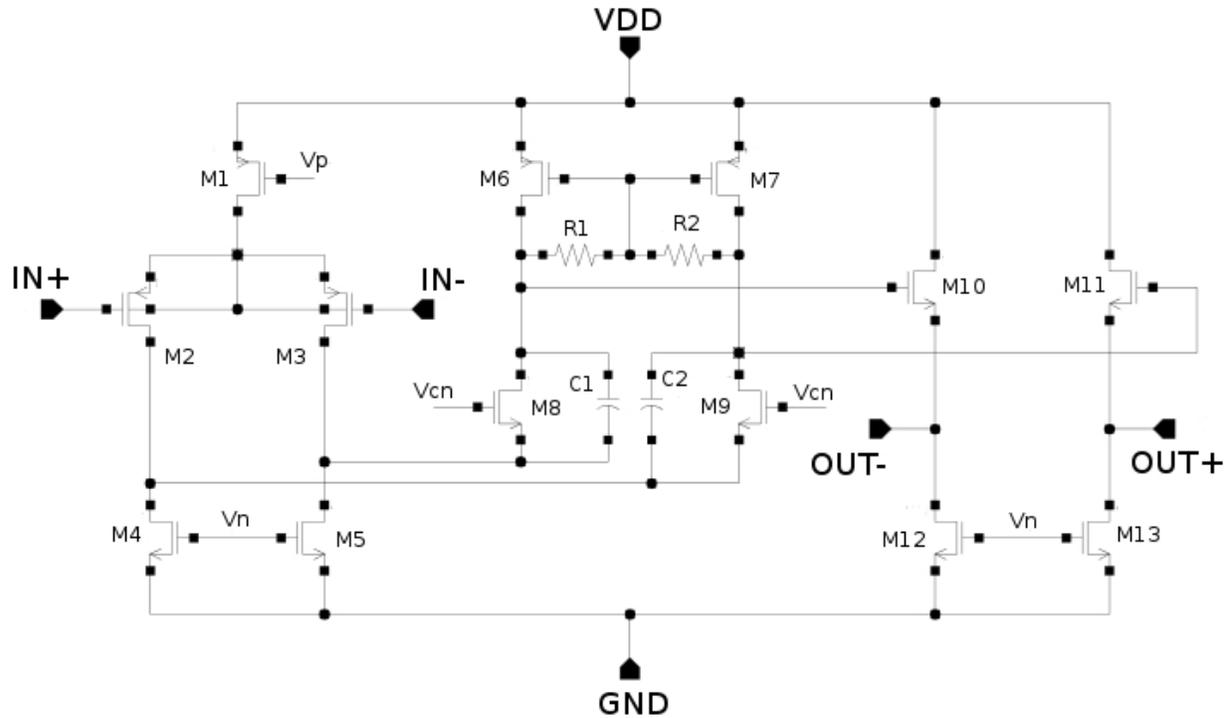


Illustration 7: Schematic of the fully-differential low-noise amplifier

M6 and *M7*. *Vp*, *Vn*, and *Vcn* are bias nodes and are connected to an on-chip bias circuitry. The detectors will be connected to the input of the amplifier as a single-ended signal and the low-noise amplifier will be used in an open-loop fashion for the sake of versatility and to achieve maximum gain and noise performance. The output buffer is conveniently biased so that the output DC quiescent common-mode voltage is half-VDD to compensate for the lack of external common-mode feedback. DC offset cancellation techniques were not implemented due to time constraints. Extra versatility was considered in the design and off-chip access to specific connections (for experimental/prototype purposes only) of the low-noise amplifier was provided in case additional compensation is necessary to avoid instant saturation of the LNA resulting from intrinsic unbalances and large open-loop gain.

4.3 Passive Switching Mixers

Illustration 8 is the schematic of one mixer. A passive switching mixer is used for the advantage of a lower $1/f$ corner, no DC bias, high dynamic range, and maximum linearity, compared to active mixer circuits^{[17]-[20]}. The disadvantages of passive mixers are compensated by the gain and low-noise of the fully-differential low-noise amplifier^[21]. These disadvantages include a slightly higher noise figure and conversion loss compared to active mixers. *RF* and *RF_BAR* connections on all four mixers are connected to *OUT+* and *OUT-* of the low-noise amplifier respectively. The structure of the passive mixer is equivalent to a single-pole double-

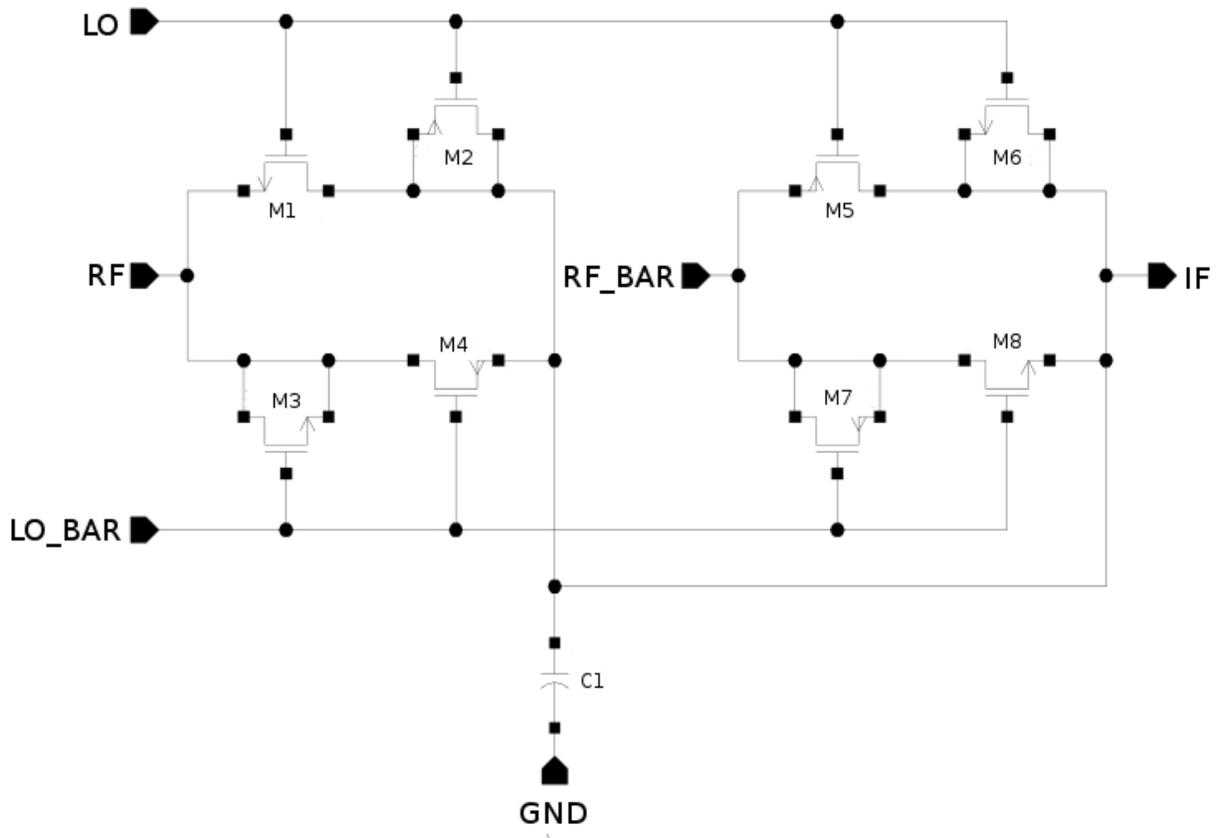


Illustration 8: Schematic of one passive switching mixer

throw switch, which switches between the 0 and 180 degree RF signals to the IF side according to the LO frequency. A pair of back-to-back transmission gates was used as the switch, where $M1 - M4$ and $M5 - M8$ are the two switches. LO feed-through cancellation techniques was also designed to reduce the effects of parasitic capacitance in the transmission gates and to optimize for linearity. Feed-through cancellation is done through the use of complementary “dummy” MOSFETs (metal-oxide field effect transistor) acting as capacitors. For example, $M3$ is $M1$'s dummy capacitor and $M2$ is $M4$'s dummy capacitor. Both the actual switching transistor and the complementing dummy transistors are identical, matched devices. The idea is that the feed-through of a rising LO edge in the switching transistor would be canceled by the falling LO_BAR edge in the complementing dummy transistor simultaneously ^[22]. The effectiveness of this LO feed-through cancellation technique is dependent on the signal quality of the LO and LO_BAR signals and the matching between all eight transistors per mixer. The layout of the mixer was constructed such that they are all symmetrical about a common stripline that is used to conduct the IF signal. A common stripline trace is used as the IF to reduce parasitic capacitance between ground and other signals because switching mixers are notorious for their strong harmonic content in the IF . A MOS-capacitor of 500fF ($C1$) is also distributed below the IF

stripline in the substrate that acts to suppress any high-frequency ringing and transients that was not canceled in the dummy capacitors. The optimal value of the suppressing capacitor was found through parametric simulation.

4.4 I/Q Differential Amplifiers (Baseband Amplifiers)

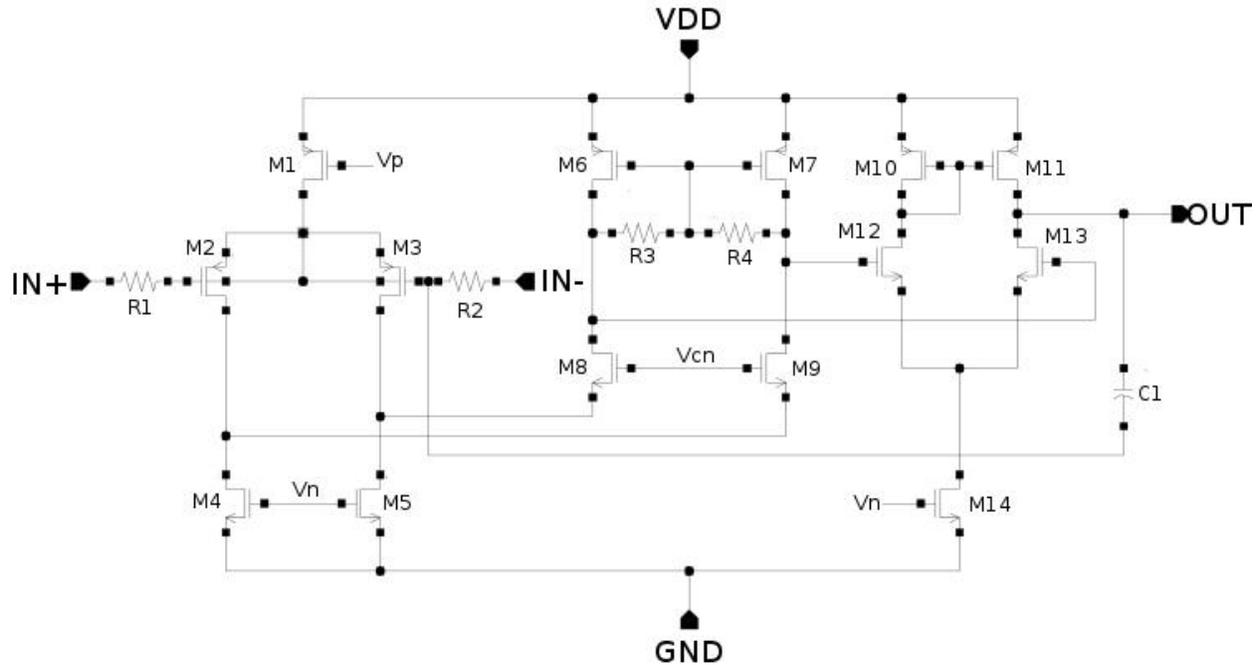


Illustration 9: Schematic of one baseband amplifier

Illustration 9 is the schematic of the baseband amplifiers that act to convert the differential I and Q signals to single-ended I and Q signals and to filter out the AC components of the mixers. The design of the baseband amplifier is an adaptation from the low-noise amplifier with the addition of a second gain stage and feedback circuitry for operation as an operational amplifier. The design of the low-noise amplifier was used as a starting point because of the limited time available. The baseband amplifier is optimized for gain and stability rather than bandwidth and low-noise. Capacitor $C1$ acts as an on-chip one-pole lowpass filter that is mounted in parallel with the off-chip feedback resistor. Additional filtering can be added off-chip. $R1$ and $R2$ are part of the feedback network for operation as a difference amplifier. The remaining feedback resistors are intentionally left off-chip due to their large chip area and versatility. The baseband amplifiers share the bias circuitry with the LNA.

4.5 Quadrature Clock Divider

Illustration 10 is the logic-level and gate-level schematic of the quadrature clock divider. A frequency divider is used to obtain synchronized clock signals of 0, 90, 180, and 270 degree phases from one master clock. Using four discrete clock sources is not employed and is not a

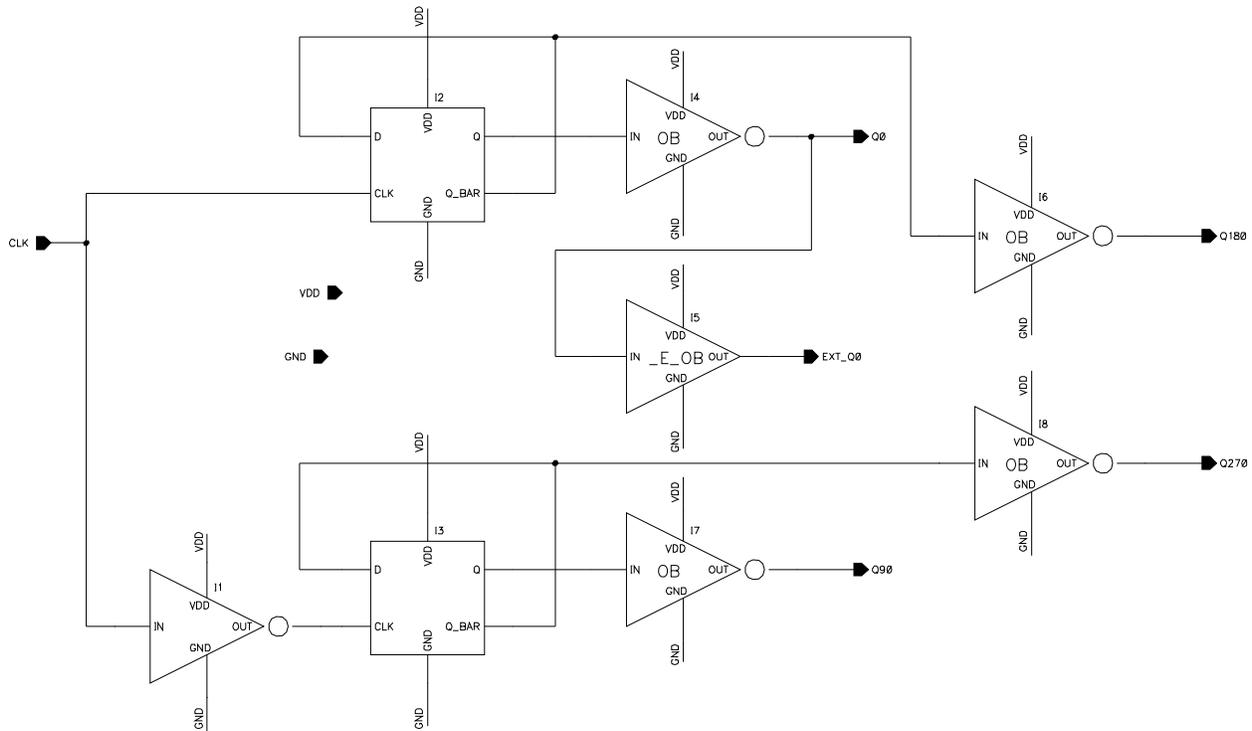


Illustration 10: Schematic of the quadrature clock divider.

good idea because it would not necessarily guarantee identical harmonic content and synchronization of each clock source. This circuit operates with an external 50% duty cycle square wave at the “CLK” (master clock) input with a frequency equal to $2f_{REF}$. The design of the frequency divider is made to be as symmetrical as possible to minimize phase errors. *I2*, a positive-edge D-type flip-flop, directly divides this signal by two down to a frequency of f_{REF} while maintaining 50% duty cycle. The output of *I2*, “Q” and “Q_BAR”, and are chosen to represent the 0 degree and 180 degree phases of f_{REF} respectively. Meanwhile, *I1* shifts the $2f_{REF}$ input clock by 180 degrees prior to frequency division. Thus, with respect to the 0 degree output of *I2*, the outputs of *I3* are the 90 and 270 degree phases of f_{REF} for “Q” and “Q_BAR” respectively. For example, a 20MHz (“ $2f_{REF}$ ”) square wave at the input “CLK” would yield four 10MHz (“ f_{REF} ”) clock signals that are shifted by 0, 90, 180, and 270 degrees.

I1 is optimized for speed and minimal propagation delay to reduce phase errors at the output. All inverters that are labeled as “OB” (*I4*, *I6*, *I7*, and *I8*) are output (inverting) buffers that are, unlike *I1*, optimized for drive capability due to the parasitic capacitance between the frequency divider and the mixers. The buffer labeled “_E_OB” (*I5*) is used to provide additional drive capability for driving off-chip circuitry. This is needed because this signal is used as the reference frequency for the terahertz setup (“Ref” in *Illustration 3* and “Reference Signal Out” in *Illustration 6*) and thus it needs to be able to drive off-chip loads. Notice that all the output

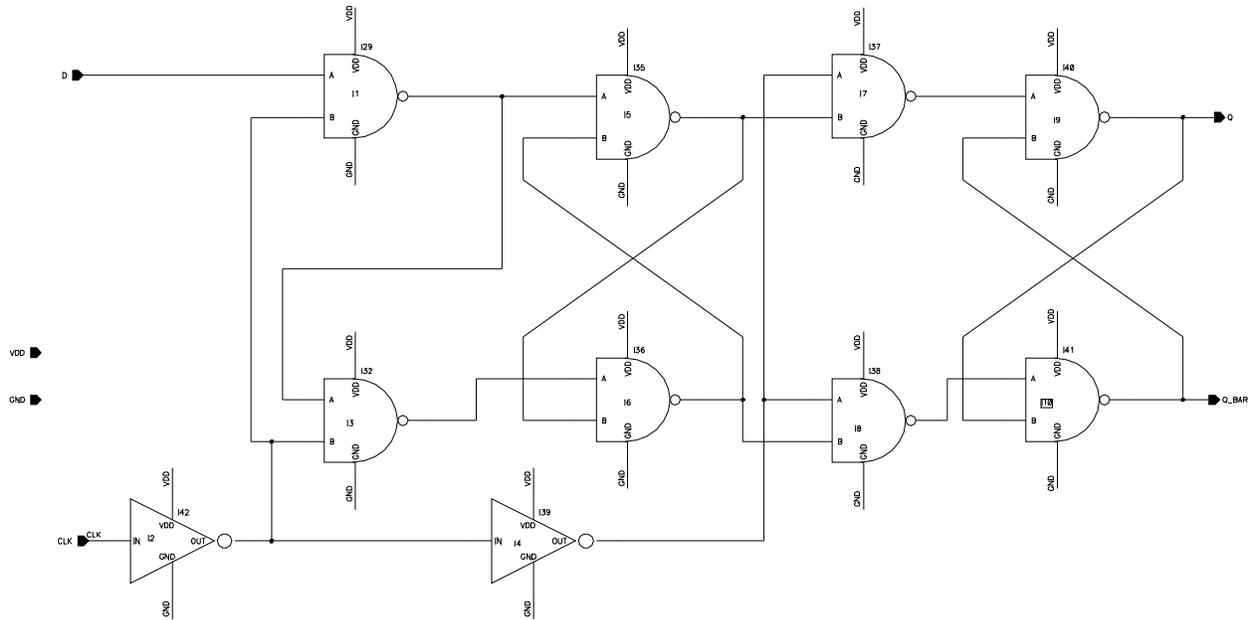


Illustration 11: Schematic of the positive-edge D-type flip-flop that is used in the quadrature clock divider.

buffers are inverting, however, orthogonality is still maintained at the outputs with respect to the 0 degree phase output “Q0”.

Illustration 11 is the gate-level schematic of the flip-flops used in the divider circuit (I2 and I3 in Illustration 10). This circuit will not be explained in detail since it is a standard circuit used within the field of VLSI design. It is shown only for reference. All gates in this circuit is optimized for speed and minimal propagation delay.

All logic gates used within the frequency divider are designed using standard schematics utilizing the complementary action of current sourcing and sinking via PMOS and NMOS transistors respectively. The transistors are sized appropriately so that the switching voltage of a PMOS and NMOS pair (i.e. inverter) is $\frac{1}{2}VDD$.

5 Results & Analysis

The chip was recently returned from the fabricating company and is currently being wirebonded to circuit boards for testing. The date of chip testing is expected to be around mid-December. Illustration 12 shows the screenshot layout of the chip in Cadence Virtuoso. The dimensions are approximately 1.5mm by 0.7mm. The green and blue rectangular areas, with the exception of the interlaced yellow/blue areas, are discrete wirebonding pads to provide electrical connections to external circuitry. The four interlaced yellow/blue areas are the ground plane structures for the 860 GHz patch antennas. In the screenshot, the patch antennas are barely visible against the yellow/blue background. The output of the diode is connected to its own dedicated wirebonding pad where the signal is extracted and where DC diode bias is

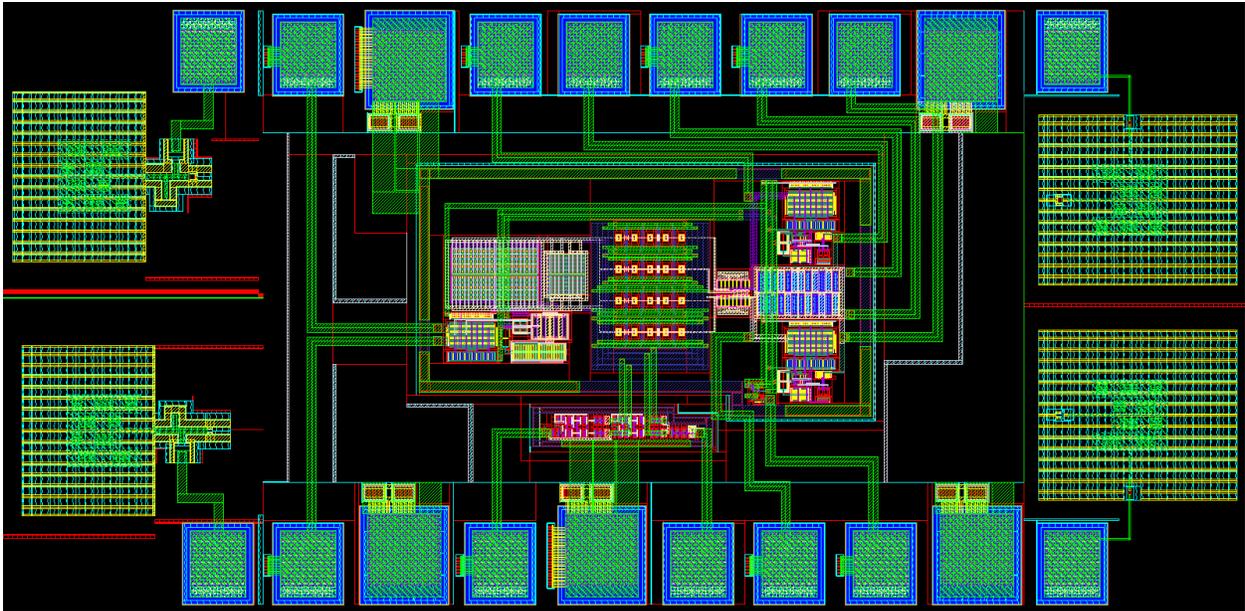


Illustration 12: Screenshot of the chip layout in Cadence Virtuoso. Bright green represents the top metal, blue is the polysilicon, and red is the silicon active area. Other layer and color definitions cannot be described because the technology information for this particular CMOS process is intellectual property (IP) of the fabrication company. A non-disclosure agreement (NDA) was made between the designer and the fabrication company under the terms that technology information cannot be released.

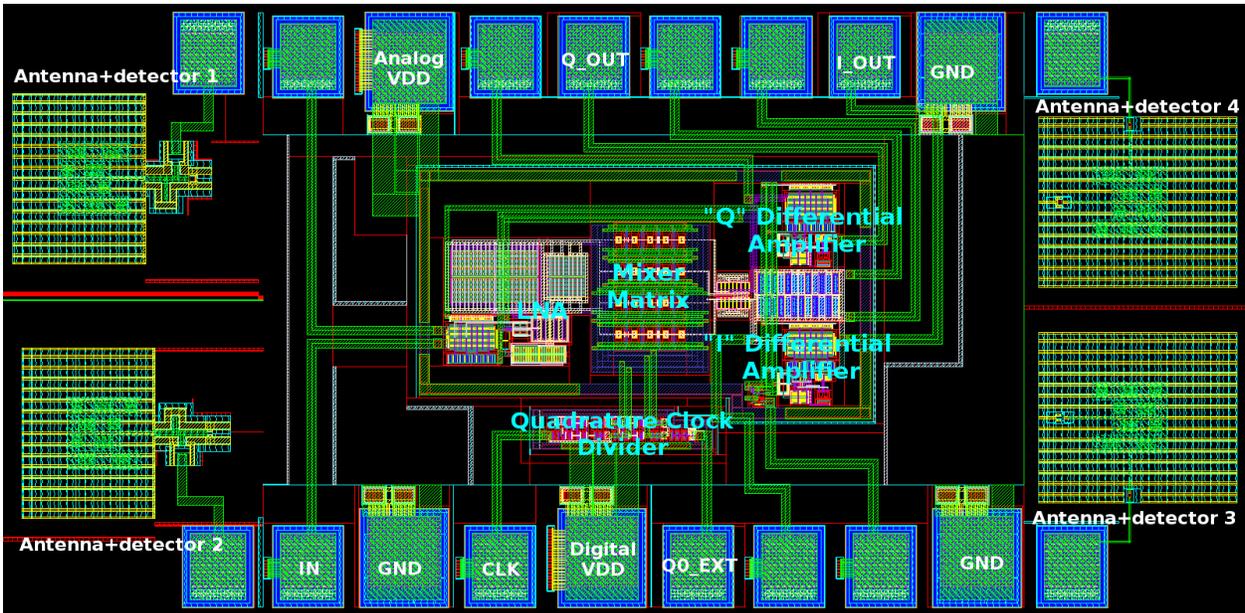


Illustration 13: annotated version of Illustration 12. Annotations are in white and sky blue bold text.

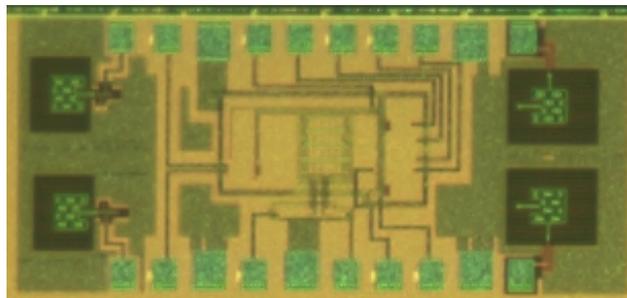


Illustration 14: Microscope photograph of the chip prior to wirebonding.

applied. The Schottky barrier diode itself is barely visible in the screenshots. Note that this is a highly experimental chip; for example, the array only has four pixels and the detector outputs are not directly connected to the lock-in amplifier. Thus, one might think the use of an off-chip capacitor is actually feasible and a differential dual-phase design is not necessary. The reason for such “unrealistic testing condition” is because since this is the first tapeout (chip version) for the lock-in amplifier, so it is more important to take small steps and to precisely prove the functionality of the lock-in amplifier itself before demonstrating the lock-in amplifier's application towards terahertz detection. Once the performance of the lock-in amplifier is verified, then it can be applied to much larger detector arrays with many more pixels. In that case, the output of each detector will have to be internally directly connected to the lock-in amplifier and the dual-phase differential design will be necessary.

Illustration 13 is the annotated version of *Illustration 12*. Note that the fully-differential low-noise amplifier block is abbreviated as “LNA” in the annotation text. The pads that are not annotated with text are strictly for experimental purposes and are only used to optimize the design and performance of the lock-in amplifier for the next tapeout. For example, some pads are used to fine-tune specific bias voltages and others are used to adjust the internal lock-in amplifier gain. These wirebonding pads are temporary and will be removed once the design of the lock-in amplifier is finalized.

Illustration 14 shows the actual chip after fabrication but before wirebonding. Note that the majority of the lock-in amplifier area is not visible and only appears as a solid color. This is partly because the fabrication company placed dummy metal patterns on the top layer of metal in specific areas to satisfy their metal density design rules. However, note that the outline of the mixer matrix and quadrature clock divider is somewhat visible. Also note that the antennas are clearly visible. The four patch antennas can be seen as bright green rectangles inside a larger, dark green rectangles (its respective ground planes). A dummy block layer was added in the antenna areas during the layout to ensure that no dummy metals would be added in this area that would otherwise effect the electromagnetic parameters of the antenna.

The Cadence/Spectre simulations of the chip as a whole are provided as preliminary results. Two important aspects are simulated: lock-in behavior and immunity to DC voltages at the input. The former is more important due to the transition from a conceptual theory to an actual device and to fulfill its main purpose as a lock-in amplifier to improve the SNR. Additionally, basic chip metrics are provided based on the simulation results.

5.1 Lock-in Behavior

Spectre's periodic steady-state (PSS) and periodic transfer function (PXF) simulations

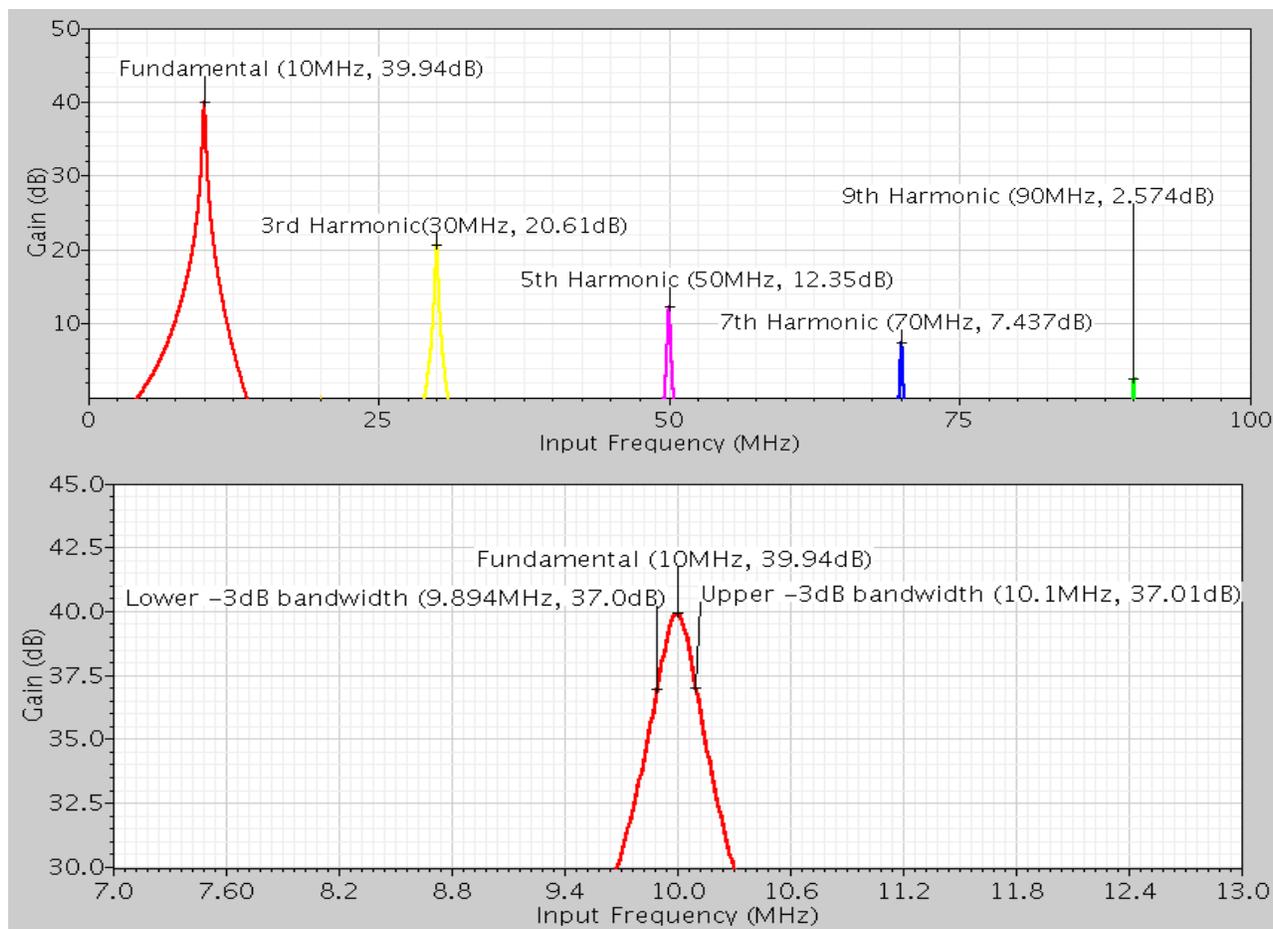


Illustration 15: (top) PSS/PXF simulation results showing the transfer function between input frequency versus effective lock-in amplifier gain. (bottom) Detailed close-up of the fundamental tone from the top graph.

were performed to graph the input frequency versus lock-in amplifier gain. PSS and PXF were used instead of standard AC analysis because of time-dependent devices such as the switching mixers. Simulation conditions are as stated: 20MHz at the “CLK” input, input sine wave with an amplitude of 1mVp-p and frequency of 10MHz, internal gain of approximately 70dB, and internal lowpass filter -3dB bandwidth of 100kHz. Recall that the clock divider divides the frequency of the master clock (input at “CLK”) by two. Thus, the 20MHz master clock is used to obtain the 10MHz lock-in amplifier clock signals used to switch the mixers and also used as the reference clock. The internal gain of 70dB is derived by adding the decibel gain of the fully-differential low-noise amplifier at 10MHz, the gain of the I/Q differential amplifier at DC, and subtracting the conversion loss of the mixer at 10MHz. The gain of the I/Q differential amplifier is expressed at DC because the DC level is the signal of interest once after direct conversion is performed.

Illustration 15 shows the PSS/PXF simulation results. Note that the frequency response of any standard fixed-gain amplifier (ideal “gain block”) would ideally have a flat line and roll off at its -3dB bandwidth. A lock-in amplifier would ideally have a sharp point of gain at f_{REF} while attenuating all other frequencies. Observe that the transfer function between input frequency

and lock-in amplifier gain is not like an ideal gain block but more of a “frequency-selective gain block” (bandpass filter). Odd-order harmonics are present in the transfer function because of the harmonic content of the square wave reference signals that drive the mixer's LO signal. Although not shown in the top graph, the gain eventually flattens out to approximately -100dB where the input frequency is not an odd multiple of f_{REF} . Most importantly, the simulation proves that this lock-in circuit follows the lock-in amplifier expression $f_{REF} \pm f_{LOWPASS}$. Simulation gives an overall gain of 40dB instead of the expected 70dB because the lock-in amplifier measures the V_{RMS} of the signal (according to *equation 1* and *equation 4*), which is slightly less than the peak amplitude of the signal. Further simulations also show that the overall leakage between the clock and output, LO-IF mixer feed-through plus I/Q differential amplifier gain, is about -40dB, which confirms the effectiveness of the feed-through cancellation technique used in the switching mixers and the differential circuit architecture.

5.2 Immunity to DC voltages

A DC voltage source in series with the signal source was used to model a DC offset at the input of the LNA and a parametric sweep was done on the PSS/PXF data with DC voltages of 0V to 10mV. The circuit was not as immune as expected (relative to the data in *Table 1*). The gain of the fundamental tone decreased by 20dB at an input DC voltage of 10mV. This is hypothesized to be most likely caused by the design of the low-noise amplifier according to the simulation. The lack of external common-mode feedback meant that the low-noise amplifier is not optimized to be driven at other common-mode voltages on the output other than the common-mode voltage dictated by the biasing. As a result, the output signal of the low-noise amplifier was being distorted in the time domain.

5.3 Other Performance Metrics

Other circuit parameters from simulation results during the design process is provided below. Simulation accurate for room temperature operation.

Highlights			Fully-Differential Low-Noise Amplifier		
Total chip area	1.13	mm ²	-3dB frequency	8	MHz
Area occupied by the lock-in amplifier only (approximate)	0.16	mm ²	Open-loop gain	20	dB
Operating voltage (VDD)	1.2	Volts	Gain at 10MHz	16	dB
Quiescent current	3.11	mA	Input referred noise	3.8	nV/\sqrt{Hz}
Lock-in maximum operating frequency	10	MHz	Phase margin	70	degrees
On-chip lowpass filter -3dB bandwidth	100	kHz	Specified input and output common-mode voltage	550	mV

I/Q Differential Amplifiers			Passive Switching Mixers		
-3dB frequency [†]	100	kHz	Conversion loss	6.7	dB
Open-loop gain	60	dB			
Phase margin	100	degrees			
Internal feedback capacitor [†]	15	pF			
Internal input series resistor (R_s) ^{††}	100	Ohms			

[†] The -3dB frequency of the I/Q differential amplifiers can be optionally decreased. The -3dB bandwidth of the internal lowpass filter can be modified by adjusting the external feedback resistor and capacitor, according to $f_{-3dB} = \frac{1}{2\pi R_f (15\text{pF} + C_{EXT})}$ where

C_{EXT} is an off-chip capacitor placed in parallel with the off-chip feedback resistor R_f .

^{††} The input series resistor is used with an off-chip feedback resistor for the I/Q differential amplifier's feedback network. The internal gain of the I/Q differential amplifier can be set by using the formula $A_v = \frac{R_f}{R_s}$. For experimental purposes only.

6 Conclusion

Overall, according to simulation, the lock-in amplifier demonstrates the ability to reduce the SNR of a desired frequency. The lock-in amplifier is able to attenuate unwanted signals by 100dB while providing a gain of 70dB on the desired frequency. This is the most important attribute right now because this first proves that the lock-in amplifier is operating as what is described. Furthermore, because this is only the first version (a prototype), perfect operation beyond its main purpose is not expected.

DC immunity is not as good as expected, however this issue will be improved upon in future tapeouts. The lock-in amplifier appears to be somewhat sensitive to DC voltages at the input. DC immunity is better than a standard lock-in amplifier however worse than what is expected. Simulations show that the gain of the lock-in amplifier decreases by approximately 20dB per 10mV of DC voltage at the input of the fully-differential low-noise amplifier.

Additionally, the basic metrics of the chip and lock-in amplifier surpasses other related works in parameters such as chip area, power consumption, and maximum lock-in operating frequency^{[13][14]}.

7 Future Research

7.1 Improvements

Time was a major constraint for this tapeout and is reflected by the relatively simple designs of each circuit block. Out of the entire year that was available for this project, only approximately less than three months was allocated for the component-level design and layout of the chip. The remaining time was occupied by school, preliminary and behavioral design, learning about CMOS design and layout, and literature review. Furthermore, this tapeout is the

designer's first experience with CMOS circuit design, layout, and tapeout. Improvements towards each circuit block is planned for the next tapeout.

Improving DC immunity is currently the highest priority improvement. Further simulations and debugging reveals that the lack of a common-mode feedback circuit and the moderate output impedance of the fully-differential low-noise amplifier is the prime cause. The lack of a common-mode feedback circuit significantly decreased the input common-mode range of the amplifier and is highly dependent on the internal biasing of the amplifier. When the input common mode voltage is out of the common-mode range of the amplifier, distortion and saturation occurred, hence why the gain decreased by 20dB with a DC offset as small as 10mV.

A second priority improvement is the introduction of an on-chip DC offset cancellation circuit for the fully-differential low-noise amplifier and the I/Q differential amplifier. This feature is also of importance because CMOS is notorious for high offset voltages by nature (10mV nominal). Coupled with the high gain of the amplifier, an offset voltage of 1mV is more than enough to completely saturate the amplifier, hence the purpose for off-chip access to key bias points in the layout. The use of a DC offset cancellation circuit will abolish the need for off-chip access to amplifier bias points and thus reduce the complexity and area of the chip ^[23].

A planned improvement that is not of the highest priority is the use of a Miller capacitance multiplier for the on-chip lowpass filter. Currently, a relatively large 15pF is included on-chip and it takes up a significant fraction of the lock-in amplifier area. The use of a Miller multiplier will enable the use of a significantly smaller on-chip capacitor and lower -3dB lowpass filter bandwidths. The use of a Miller multiplier will significantly increase the area usage efficiency and performance of the lock-in amplifier because, as the name suggests, a Miller multiplier can use a relatively small capacitor and increase the effective capacitance without increasing the area of the capacitor. This is done by using an inverting amplifier (can be as simple as a common-source FET amplifier) and a small capacitor. Unlike a regular capacitor, the effective capacitance of a Miller multiplier circuit can be increased only by adjusting the gain of the inverting amplifier, thus using less area per unit of capacitance and adding extra versatility to the design.

Other improvements that are relevant to the lock-in amplifier architecture but are not of importance currently include the incorporation of an analog-to-digital converter after the I/Q differential amplifier. Not only will this make the chip easier to interface with digital appliances (i.e. computers), it will also allow the use of digital signal processing on the chip. For example, the response time of the current on-chip lowpass filter is limited to its time constant. If the lowpass filter is replaced with the analog-to-digital converter and some digital circuitry, various

sampling techniques can be employed with different performance attributes can be used to act as an effective lowpass filter but yield better performance than the typical lowpass filter ^[24]. This will increase the versatility and, depending on the specific application, the performance of the chip with minimal external components.

7.2 Other Architectures

Another route to improving performance is to consider a totally new architecture. Lock-in amplifiers have specific drawbacks that may appear to be highly undesired in some applications. For example, although the lock-in amplifier does remove noise, it does not entirely remove flicker noise. This is because of the down-conversion nature of the architecture and the nature of CMOS. The flicker noise caused by the “experiment” is removed however the flicker noise that occurs within the lock-in amplifier itself is not removed.

Deviating from the lock-in amplifier architecture, a “low-IF lock-in amplifier” can be designed that will completely remove flicker noise. Instead of direct conversion, the mixers shift the signal to an intermediate frequency that is away from flicker noise and thus avoid the flicker noise entirely. This is similar to the operation of a super-heterodyne circuit used in most radio receivers. From there, an analog-to-digital converter would be necessary to convert the amplitude into a usable format. The overall noise reduction may be inferior to the standard direct conversion technique, but this solution may be appropriate if the input frequency spectrum has a low noise density (relative to the amplitude of the desired signal) but with a high flicker noise content.

A more advanced architecture is the bandpass delta-sigma analog-to-digital converter. This circuit is similar to the low-IF technique described above, however an on-chip bandpass filter is used instead of mixers and the entire circuit is placed within the feedback loop of a delta-sigma analog-to-digital converter. This architecture combines both the noise-reduction and digitizing circuits in one, thus adding extra versatility, complete removal of flicker noise, and equal (if not, better) performance compared to the standard lock-in architecture ^{[25][26]}. Currently, no published work exists yet about incorporating a bandpass delta-sigma analog-to-digital converter with a terahertz detector array on monolithic CMOS.

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