

EE6311 Final Design Project – Microwave Module Design

For your final project use AWR or ADS to design each of the microwave components that comprise one of the following modules:

- A) Transmit Channel for Phased Array Radar Module
 - SPDT Switch
 - 2-Bit Phase Shifter (90° Switched-line, 22.5° loaded-line)
 - 2-Bit Step Attenuator (5, 2 dB)
 - 2-Stage Balanced Amplifier
- B) Receive Channel for Phased Array Radar Module
 - SPDT Switch
 - 2-Bit Phase Shifter (90° Switched-line, 11.25° loaded-line)
 - 2-Bit Step Attenuator (10, 1 dB)
 - 2-Stage Balanced Amplifier
- C) Three-channel Wideband Receive Amplifier Module
 - SP3T Switch
 - 3-Bit Step Attenuator (15, 8, & 1.5 dB)
 - Three 2-stage Linear Amplifiers with non-overlapping bandwidths
- D) Feed-forward High Linearity Amplifier Module
 - Power Divider/Combiner
 - Phase Shift Bit and Coupler
 - 2-Stage Linear Amplifier
- E) Adjustable Gain Amplifier Module
 - 3-Bit Step Attenuator (15, 8, 2 dB)
 - 2-Bit Phase Shifter (90° Switched-line, 22.5° loaded-line)
 - 22-dB Coupler for output power monitor
 - 2-stage Balanced Linear Amplifier

Design Requirements:

- Each component is to be designed in microstrip on your choice of substrate material (ceramic, soft substrate, GaAs, Si, etc.). Include appropriate junction discontinuities (MSTEP, MTEE, etc.). AWR models for switches and couplers can be used.
- Active components may be FET, pHEMT, mHEMT, Bipolar or PIN diode (transistor S-parameters or equivalent circuit models can be found at vendors' websites)
- Matching elements can be lumped-element or distributed (can use AWR/ADS elements, as appropriate)
- Include bias networks for amplifiers and control elements (switches; atten, phase bits)
- Examine amplifier stability over a minimum frequency range of an octave on either side of your center frequency, f_0 .
- Frequency and bandwidth is your choice
- Layout not necessary
- Two-person teams; divide up component designs and presentation material as equally as possible

Required Slides for PowerPoint presentation:

- Title slide with project description, name, date
- Module block diagram with high-level summary specs (functions, freq, BW, gain, etc.)
- Summaries of design approach for each major component in module
- Circuit schematic and rf performance plots of each major component
- Tabular summary and frequency response plots of overall module performance (include major phase or attenuator states, dc bias voltages and currents required)
- Discuss design issues or ways you could have improved design
- Brief summary of an article from *IEEE Transactions on Microwave Theory and Techniques*, *Microwave Journal*, etc. that is a similar design to what you did. Cite reference and give 1-slide overview of what authors did that was similar. IEEE journals are free to access on “IEEE Xplore” from the UTD library. (<http://ieeexplore.ieee.org/Xplore/dynhome.jsp>)
- One hard copy of all of your slides.

This final design project will represent 50% of your Homework/Design Projects grade (or 25% of your final grade). We will begin in-class presentations on **Wednesday, Nov. 19th**. (Presentation order will be determined by random draw if no volunteers.) Three (or four) projects will be presented per class period, with the final presentation on Wednesday, Dec. 3rd. Attendance is mandatory for everyone, whether you are giving your presentation or not during that class period. Presentations by each person must be **5 minutes minimum** and **10 minutes maximum**. Grading will be based on completeness and soundness of design, creativity, and presentation (having required slides, clarity of speech, eye contact, within time limits, etc.) You may bring your own laptop or a memory stick to load on the classroom computer.

Presentations:

Nov. 19 1. Raminder and Ade
 2. Kash, Dadrian and Naqi
 3. Yat and Daniel
 4.

Nov. 24 1. Raja and Rashid
 2. Rupesh and Pankaj
 3. Payam and Sudharsan
 4. Shrenik and Sibasis

Nov. 26 1. Liam and Richard
 2. Dustin and Vikas
 3. Allan and Carl
 4. Israel and Julian

Dec. 1 1. Ben and Beatriz
 2. Jason and Joseph
 3.
 4.