

Frequency Driven Repeater Insertion for Deep Submicron

N. Ahmed, M. H. Tehranipour, D. Zhou, M. Nourani

Center for Integrated Circuits & Systems

The University of Texas at Dallas, Richardson, TX 75083

{mht021000, nxa018600, zhoud, nourani}@utdallas.edu

Abstract—Repeaters are now widely used to decrease delay and increase the performance of long interconnects. The maximum operating frequency is limited by the longest wire between two repeaters. The main goal of repeater insertion is to reduce the delay of the interconnects in a circuit. Increasing the number of repeaters on an interconnect increases the slew rate and the operating frequency but decreases the design performance in terms of area and power. This paper presents a new methodology of repeater insertion considering the circuit operating frequency to improve the slew rate and reduce the area overhead of the repeaters. We propose a mathematical treatment for finding the number and position of repeaters while keeping the same size of the optimal repeater size. Experimental results are shown for different frequencies and repeater sizes to indicate the improvements of slew rate and saving area overhead.

I. INTRODUCTION

As very large scale integration (VLSI) circuits continue to be scaled aggressively past the 130-nm technology, performance of these IC's is being increasingly dominated by the interconnects. With technology scaling, more and more functionality is being integrated on-chip which results in an increase in die size inspite of the reduction in minimum feature size. As a result, the number of long wires and the length of these wires increases. The interconnect delay is also becoming a bottleneck in achieving high performance circuits. The power consumption of the buffers inserted in interconnects is another important factor in the interconnect design. Techniques which aim to reduce interconnect delay and power consumption are required for high speed circuit design.

Repeaters are now widely used to decrease the delay and increase the performance of long on-chip interconnections in CMOS VLSI. For large high-performance designs, the number of such repeaters can be very high and can take up significant fraction of active silicon and routing area. Additionally, as the operating frequency and leakage current increases while scaling, total chip power dissipation increases. A significant fraction of the total chip power dissipation arises due to long interconnect networks, especially in high-performance designs. For example, it has been reported that around 40%-70% of the total power consumption could be due to the clock distribution network [1].

High performance VLSI circuits are designed to work at a specific maximum clock frequency depending on their applications and the process technology used. The chip frequency increases as the technology scales down [2]. One of the constraints in achieving maximum clock frequency is clock rise time (t_r). The clock frequency is limited by the longest rise time in the clocking network [3]. The slew rate is inversely related to transition time and is defined as $(V_{90\%} - V_{10\%})/t_r$ as reducing t_r increases the slew rate. The clock rate limit in a buffered clock tree depends on the phase delay and transition time of each subtree instead of that of the whole clock tree. A pipeline scheme was presented to meet the GHz frequency challenge [4]. The distribution of clock signal on the chip must be done while minimizing the clock delay and clock skew and maximize the slew rate [5].

The operating frequency has a major impact on the number of repeaters that needs to be inserted. As the number of repeaters increases, the area and power dissipation of the drivers increases. In this paper, we propose a new repeater insertion methodology for improving the slew rate and reducing the area of the repeaters considering the operating frequency. This method is performed in two steps: First, the

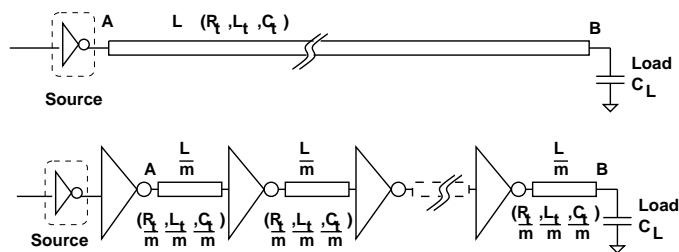


Fig. 1. Uniform Repeater Insertion.

method finds the required number of repeaters on an interconnect to satisfy the operating frequency using a uniform repeater insertion. Second, the methodology proposes a new technique of repositioning the repeaters based on uniform shifting of the repeaters to the receiving end of the interconnect. For this purpose, we present a mathematical treatment for finding the number of repeaters and their positions. The second step of this methodology increases the slew rate and decreases the area compared to the first step without increasing the delay and power.

The rest of the paper is organized as follows. Section II describes the background about uniform repeater insertion, relation between operating frequency and number of repeaters and how delay, slew rate and power varies with position of the repeaters. The uniform shifting of the repeaters is discussed in Section III. Section IV discusses the experimental results. The paper ends with conclusion in Section V.

II. BACKGROUND

A. Uniform Repeater Insertion

Consider an interconnect of length, L and width, W between the source, i.e. the output buffer of the last stage, and a load as shown in Figure 1. The propagation delay of the interconnect increases quadratically with the line length. Repeaters are inserted to change the delay dependence on the length from quadratic to linear. There are m repeaters uniformly placed on the interconnect line, whose total resistance, inductance and capacitance are R_t, L_t and C_t , respectively. Each of the repeaters drives exactly identical interconnect length and is K times larger than the minimum size balanced inverter. The total capacitive load driven by each repeater is equal to the sum of the interconnect segment capacitance (C_t/m) and the intrinsic input capacitance of the repeater (C_r). C_r is proportional to the size of the repeater.

Many analytical delay models have been developed for different repeater and interconnect models [6][7]. To observe the effect of the repeater insertion on various parameters like phase delay and slew rate, we did SPICE simulations on an interconnect of length $L=1cm$ and width $W=1\mu m$ for different values of m and K . All simulations are performed using 0.18 μm technology. Each interconnect segment is modeled as a distributed RLC line. The R, L and C parameters are derived using Berkeley Predictive Technology Model (BPTM) [8]. The maximum voltage is 1.8V and the input rise time used is 100 ps. The input slew rate is calculated using $(V_{90\%} - V_{10\%})/(t_{90\%} - t_{10\%}) = 18V/ns$.

Figure 2 shows the delay and slew rate variation with different number of repeaters and for three different values of K . For this specific example, the optimum delay occurs at $m=1$ and gradually increases as m

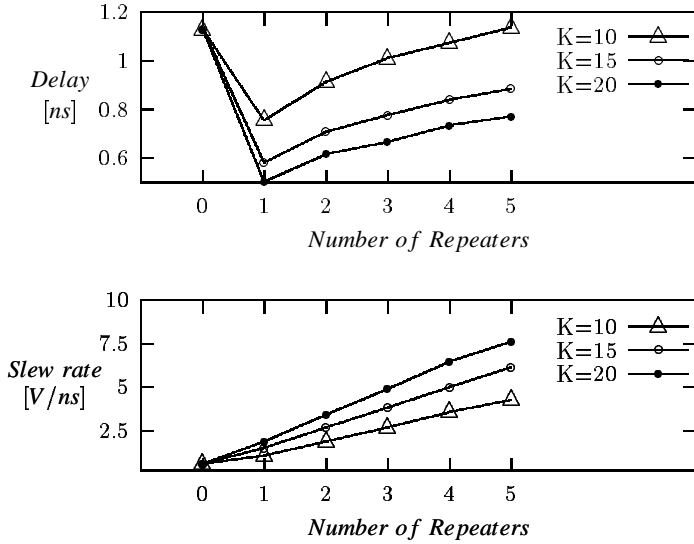


Fig. 2. Delay and slew rate variation with number of repeaters.

increases. This is because the interconnect segment delay is less than or equal to the repeater delay for $m > 2$. In such a situation, adding repeaters increases the overall delay. When the length of the interconnect increases, the number of repeaters required for optimal delay also increases. The slew rate corresponding to the optimal delay at $m = 1$ for $K=20$ is 1.865 V/ns, i.e. a transition time of 900 ps. This severely limits the maximum frequency of data transfer across the interconnect. A higher transition time implies higher switching time which relates to more short circuit power dissipation. The transition time can be decreased by either increasing m or K . The number of repeaters are selected depending upon the delay and power specifications to obtain a better slew rate. In the next subsection, we discuss about repeater insertion with considering the frequency.

B. Relation Between Frequency and Number of Repeaters

The operating frequency also impacts on the number of repeaters to be inserted. We show a relation between them and develop a formulation to find the number of repeaters to be inserted for a given operating frequency. Figure 3 shows the output waveforms for different number of repeaters for an input signal frequency of 1GHz for an interconnect with $L = 1\text{cm}$ and $W = 1\mu\text{m}$. The size of the repeaters is $K = 20$. Even though $m = 1$ gives optimum delay, the output waveform does not reach the full voltage swing of 0 to 1.8V. As m increases, the slew rate improves and the output gets better in shape and pulse width. Depending on the slew rate constraint, the designer can choose $m \geq 3$ for the above design to work at 1GHz. It is clear that as the operating frequency increases, the number of repeaters also increases.

There is a limit to how long a wire can be in between two repeaters at a certain frequency. The maximum clock rate in a buffered clock tree running in pipeline scheme is formulated in [4]. Applying it to a single interconnect line, the clock rate limit is given by:

$$f_{pipe} = \frac{1}{2(\tau_{p_{max}} + \tau_{t_{max}} + \tau_h)}$$

$$\tau_{p_{max}} + \tau_{t_{max}} \leq \frac{T_{period}}{2} - \tau_h$$

Assuming a uniform placement of repeater insertion $\tau_{p_{max}}$, $\tau_{t_{max}}$ and τ_h are the phase delay, transition time ($V_{50\%}$ to $V_{90\%}$) and specified

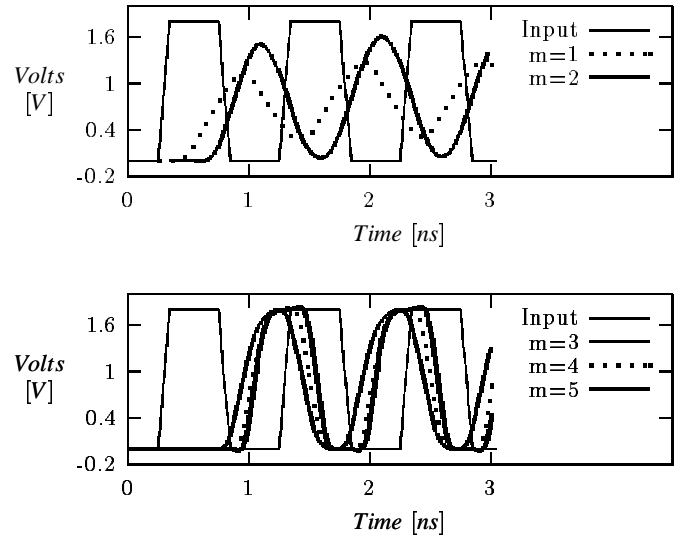


Fig. 3. Output waveforms for an input signal frequency of 1GHz.

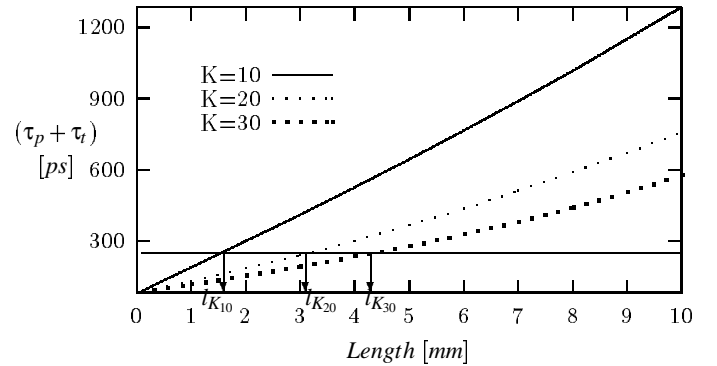


Fig. 4. Variation of $(\tau_p + \tau_t)$ with length of the interconnect for different size factors K

holding time of a sub-segment between any two repeaters, respectively. For a given slew rate or holding time constraint, the maximum length of wire between two repeaters can be found.

Elmore delay model provides a good approximation for 50% delay but there is not much accuracy for 10% and 90% points of the output waveform. We perform SPICE simulations for a range of interconnect lengths between different inverter sizes. Figure 4 shows the variation of $(\tau_{p_{max}} + \tau_{t_{max}})$ with length for different K . For a holding time constraint of $25\%T_{period}$, the maximum length of wire between two repeaters of size $K=10$, $K=20$ and $K=30$ are 1.5mm, 3.1mm and 4.2mm, respectively. The number of repeaters of size K to be inserted in an interconnect of length L is determined by $m \geq \frac{L}{l_{K_{max}}}$, where $l_{K_{max}}$ is the maximum length of wire between two repeaters of size K . For example, for $l=1\text{cm}$ and $K=20$, $m \geq 3.23$, meaning $m=4$ is the best choice to satisfy the operating frequency. Compared to the uniform repeater insertion, the required number of repeaters is increased when the frequency is considered. However, the main goal is to insert as less repeaters as possible to satisfy the frequency.

C. Relation Between Position of Repeaters and Slew Rate

The simulation results explained in the previous section for uniform repeater insertion suggest that in order to obtain a better slew rate either m or K is to be increased. In this section, we show a relationship between the position of the repeaters and the slew rate. This relationship

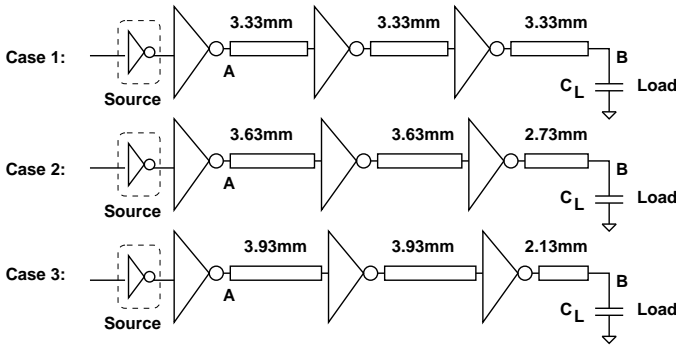


Fig. 5. 3-stage repeaters with different positions with $K=20$.

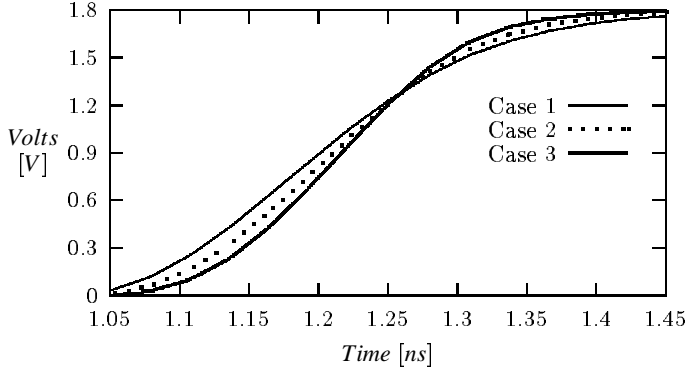


Fig. 6. Output waveforms for different positions in a 3-stage repeater.

will be the foundation for further discussion on how to improve the slew rate by adjusting the position of the repeaters instead of increasing m or K . Figure 5 shows an example with three repeaters of size-factor $K=20$ inserted on an interconnect of length $L=1cm$ and width $W=1\mu m$. There are three different cases with repeaters placed in different positions. *Case1* shows the uniform repeater insertion. In *Case2* and *Case3* the second and third repeaters are equally shifted towards the load end by a fixed amount of $0.3mm$ and $0.6mm$, respectively.

Figure 6 shows the output waveforms at B for the three different cases for $f=1GHz$. Clearly, the slew rate increases as the repeaters are shifted to the load end of the interconnect. By shifting the repeaters, the segment length driven by the first two repeaters is increased. As a result, the delay of these segments is increased. This increase in delay is compensated by the decrease in delay and transition time in the final segment. The overall delay in the shifted case is slightly greater than in uniform placement. With well defined buffer size and positioning, the slew rate can be improved.

Table I compares the three different cases in terms of phase delay, slew rate and power dissipation. The slew rate is improved by 33% in *Case3* compared to uniform repeater insertion at a cost of 2.5% increase in phase delay. The power dissipation is increased by 2.4%. As mentioned before, $m=4$ is the best choice for an interconnect of length $L=1cm$ and width $W=1\mu m$ operating at $f=1GHz$. The last row in the table shows the parameters for $m=4$. It is clearly seen that *Case3* ($m=3$) gives better performance in terms of delay, slew rate and power compared to the uniform placement with $m=4$. Based on these simulation results, a lower number of stages can improve the slew rate and power by adjusting the position of the repeaters, thereby saving area and power.

III. UNIFORM SHIFTING OF REPEATERS

Uniform repeater insertion is used to find the number of stages and repeater size to obtain optimal delay when driving interconnect load.

TABLE I
COMPARISON OF PHASE DELAY, SLEW RATE AND POWER FOR DIFFERENT POSITIONS OF REPEATERS.

	t_d [ps]	SR[V/ns]	P_{diss} [mW]
$m=3$, Case 1	653.2	5.7	4.412
$m=3$, Case 2	661.9	6.5	4.459
$m=3$, Case 3	669.4	7.6	4.517
$m=4$, Uniform	719.3	7.4	4.685

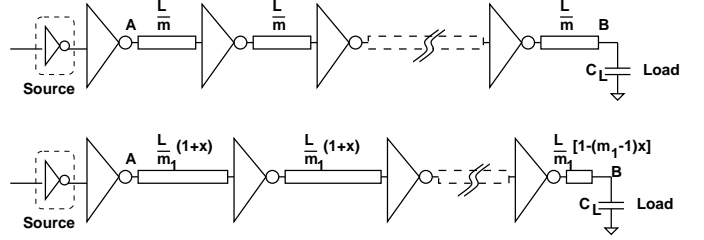


Fig. 7. Uniform shifting of repeaters (size factor K).

Sometimes optimal delay may not satisfy the design specifications. Other parameters like transition time and power are also important. As seen in Section II-A, the corresponding transition time for optimal delay was high which limited the maximum operating frequency. Instead of increasing the number of repeaters, suitable position of repeaters can be determined to improve the performance. In this section, we propose a technique to find the number of repeaters lesser than uniform repeater insertion for a given operating frequency and their positions to obtain the same performance.

The first step is to perform uniformly placed repeater insertion to meet the design constraints. This can be done in two different methods. In the first method, the repeater size and the number of repeaters can be calculated by finding an analytical expression for $(\tau_p + \tau_r)$ and embedding it in the formulation discussed in Section II-B. The second method is to do a prior SPICE analysis and find the number of repeaters satisfying delay and power requirements, for a given frequency of operation. In our design methodology, we apply the latter method. In the next step, we determine the number of repeaters and the amount of shift to decrease the area.

Figure 7 shows two circuits with different repeater insertion methods for an interconnect of length L . In the first circuit, m repeaters with size factor K are uniformly placed along the interconnect. Noticing that the slew rate improves by shifting the repeaters to the receiving end, we select m_1 uniformly placed repeaters ($m_1 < m$) and shift them by a fixed factor x . The size factor of the repeaters in both circuits is the same.

A. Determination of parameter x

Each repeater stage is shifted by a fixed factor x towards the load end except the first repeater. The first $(m_1 - 1)$ segment lengths are increased by factor x and the last segment length is reduced by a factor of $(m_1 - 1) \times x$.

$$l_i = \begin{cases} \frac{L}{m_1}(1+x) & 1 \leq i \leq (m_1 - 1) \\ \frac{L}{m_1}[1 - (m_1 - 1)x] & i = m_1 \end{cases}$$

Assuming the length of the last segment to be β times the segment length without shift, where $0 < \beta \leq 1$. Equation 1 shows x in terms of β and m_1 . When $\beta = 1$, x becomes zero which implies uniform placement of repeaters.

$$l_{m_1} = \frac{L}{m_1}[1 - (m_1 - 1)x] = \beta \times \left(\frac{L}{m_1}\right)$$

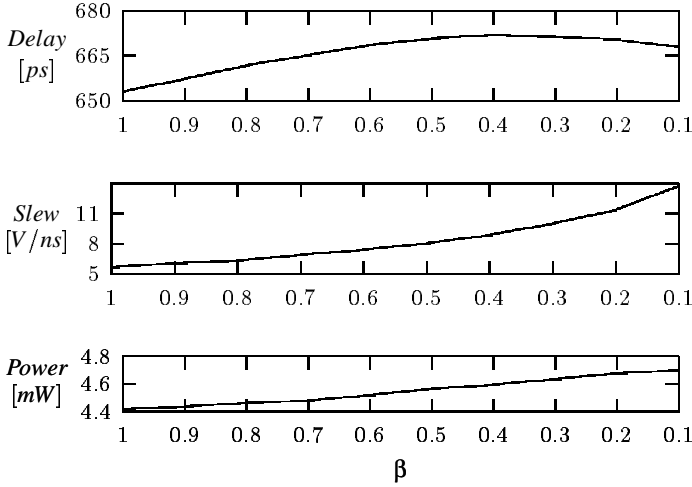


Fig. 8. Variation of delay, slew rate and power with β .

$$x = \frac{(1 - \beta)}{(m_1 - 1)} \quad (1)$$

Figure 8 shows the variation of delay and slew rate with β for three repeaters inserted on an interconnect of length $L = 1\text{cm}$ and width $W = 1\mu\text{m}$. When β is decreased, x increases and so the amount of shift. The delay of the first $(m_1 - 1)$ segments increases because the load driven by the repeaters increases. The delay reaches a maximum when $\beta = 0.4$ and gradually falls with decrease in β . This is because the decrease in delay in the last segment starts to dominate the sum of the increase in delays for the initial $(m_1 - 1)$ segments and the overall delay decreases. The slew rate and power continuously increase as the load driven by the last repeater decreases as β decreases. It is clear that in order to obtain a significant improvement in slew rate and meet the delay and power lower than the case of $m=4$ (as shown in Table I), the value of β must be chosen between 0.2 and 0.5 ($0.2 < \beta < 0.5$). From Equation 1, x can be expressed by the inequality $x > \frac{1}{2(m_1 - 1)}$ and then

$$x \simeq \frac{1}{m_1} \quad (2)$$

We choose $x = 1/m_1$ which satisfies this inequality.

B. Determination of parameter m_1

As seen in Figure 7, the repeater size is the same in both the circuits. Therefore, in order to obtain a better slew rate, the length of the segment driven by the final repeater after applying shift should be less than the segment length driven in uniformly placed circuit. This can be expressed as:

$$\frac{L}{m_1}[1 - (m_1 - 1)x] < \frac{L}{m}$$

Substituting Equation 2, m_1 is determined by the inequality $m_1 > \sqrt{m}$. Due to shifting, the length of first $(m_1 - 1)$ segments increases. There is a limit on the length of interconnect ($l_{K_{max}}$) between two repeaters for a given operating frequency as explained in Section II-B. If the segment length exceeds $1.5 \times l_{K_{max}}$, $(\tau_p + \tau_t)$ is close to $\frac{T_{period}}{2}$, the output waveform degrades and has a triangular shape.

$$\frac{L}{m_1}(1 + x) < 1.5 \times l_{K_{max}} \quad \text{where } x = \frac{1}{m_1}, m = \frac{L}{l_{K_{max}}}$$

Combining the two inequalities, the limit of m_1 can be expressed as:

$$\max\left\{\sqrt{m}, \frac{m + \sqrt{m^2 + 6m}}{3}\right\} \leq m_1 < m$$

TABLE II
COMPARISON OF UNIFORM PLACEMENT AND UNIFORM SHIFT METHODS
FOR OPERATING FREQUENCY $F=1\text{GHz}$ AND 2GHz .

Frequency	K	Repeaters	Area	Delay [ps]	SR [V/ns]	Power [mW]
f= 1GHz	20	m=4, Uniform	80	719.3	6.55	3.73
	20	m=3, $\beta = 0.4$	60	673.7	6.85	3.54
f= 2GHz	27	m=6, Uniform	162	654.6	13.3	10.65
	27	m=5, $\beta = 0.4$	135	625.1	15.1	9.62

IV. EXPERIMENTAL RESULTS

Table II compares the results of uniform placement of repeaters and fixed shifting of repeaters for two operating frequencies. The length of the interconnect $L = 1\text{cm}$ and width $W = 1\mu\text{m}$. As the operating frequency increases, the number of repeaters required and the size factor increases. The hold time (τ_h) constraint used is $25\%T_{period}$ which implies a $(\tau_p + \tau_t)$ period of 250 ps and 125 ps for operating frequency $f = 1\text{GHz}$ and $f = 2\text{GHz}$ respectively. The input rise time used is equal to $10\% \times T_{period}$. For the same performance, the number of repeaters for the uniform shift methodology is less compared to uniform placement of repeaters. The slew rate is improved by less number of repeaters, thereby saving area and power. As the technology shrinks, the operating frequency increases and the number of repeaters increases. The proposed methodology will be more effective in terms of performance for higher operating frequencies.

V. CONCLUSION

The paper proposed a new methodology of repeater insertion to improve the slew rate and reduce the area/power. The method repositions the repeaters inserted during uniform repeater insertion by a fixed shifting factor. As reported in experimental results, the new repeater insertion methodology shows better results compared to uniform repeater insertion in terms of slew rate and area/power.

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