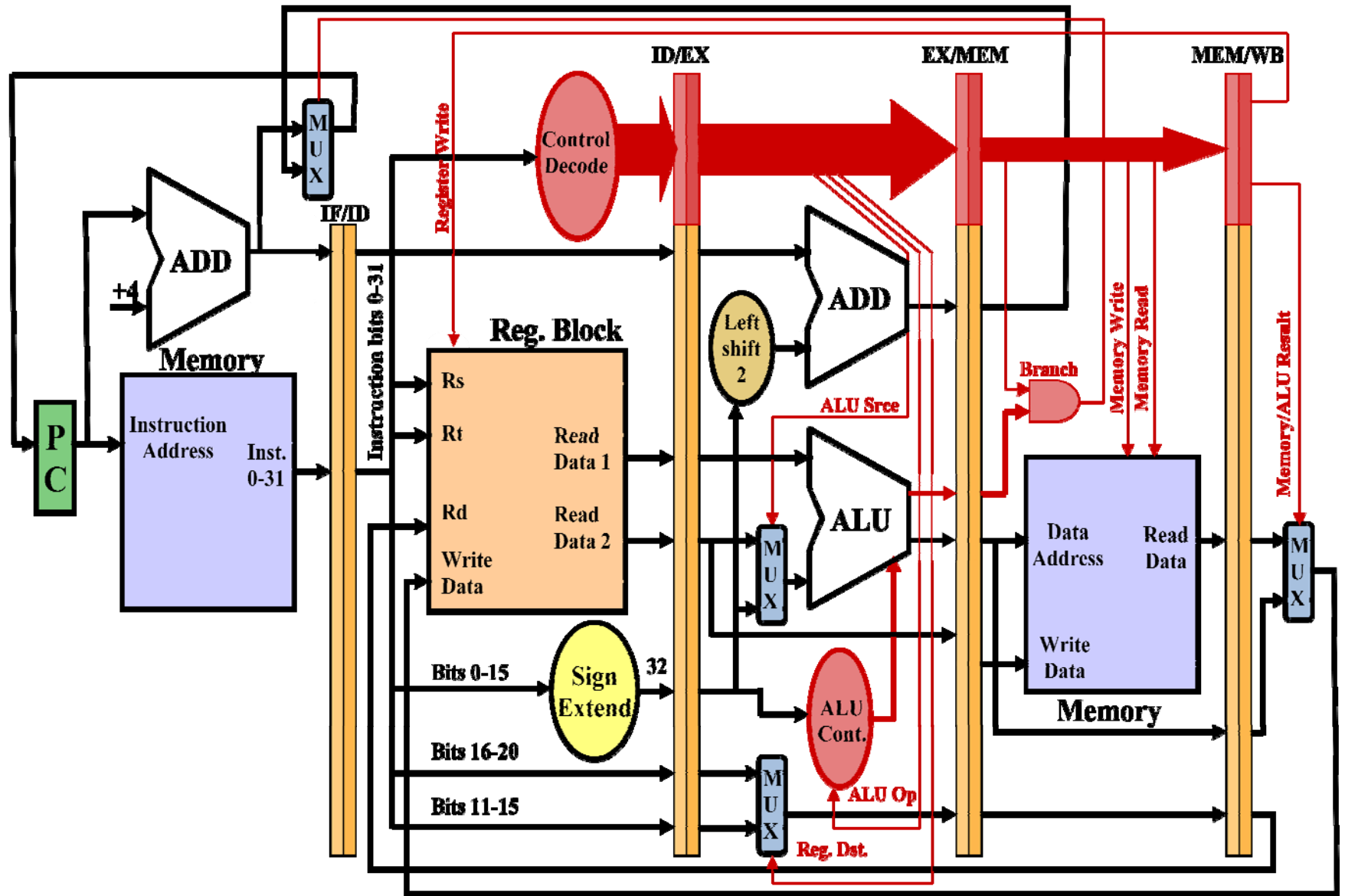
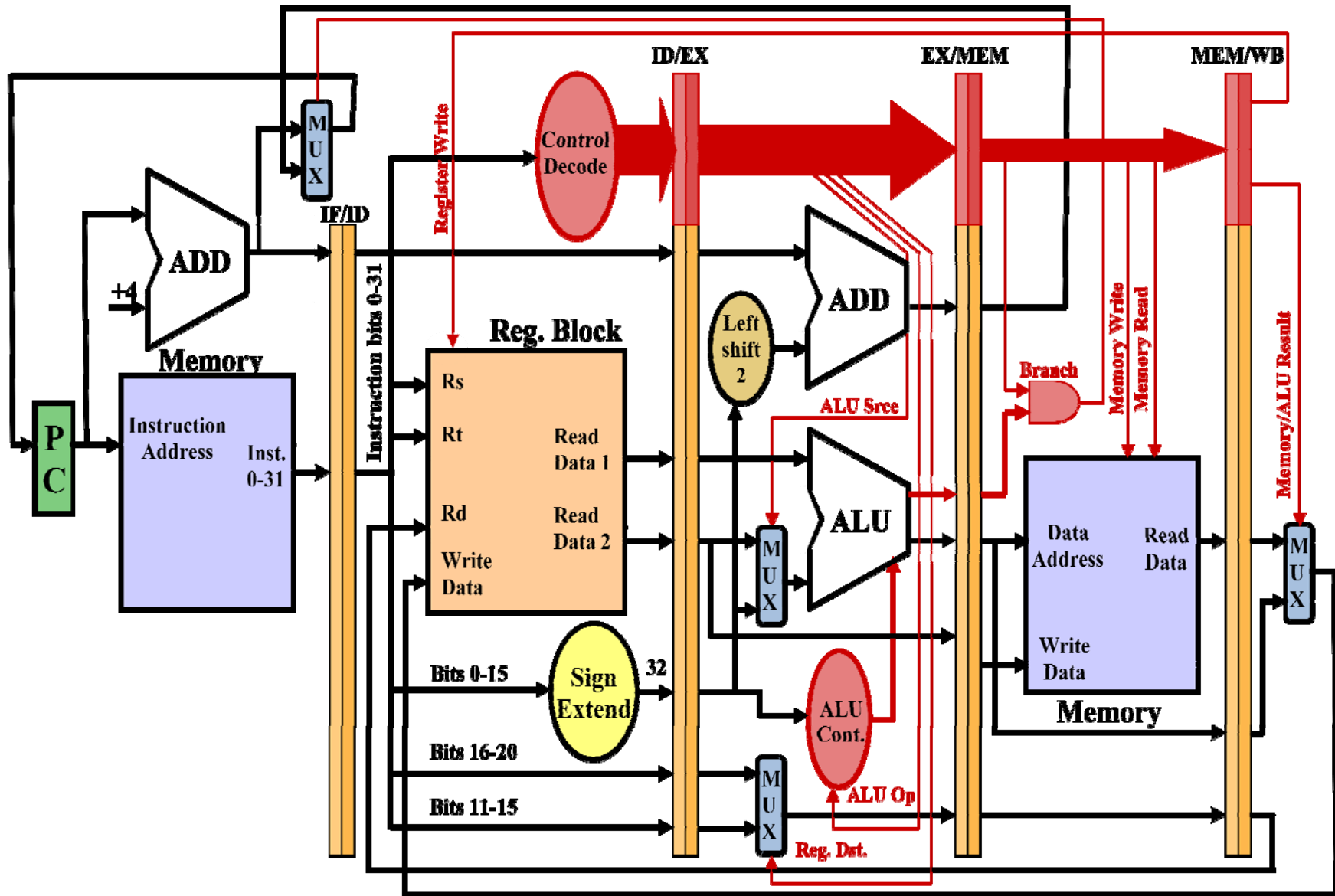


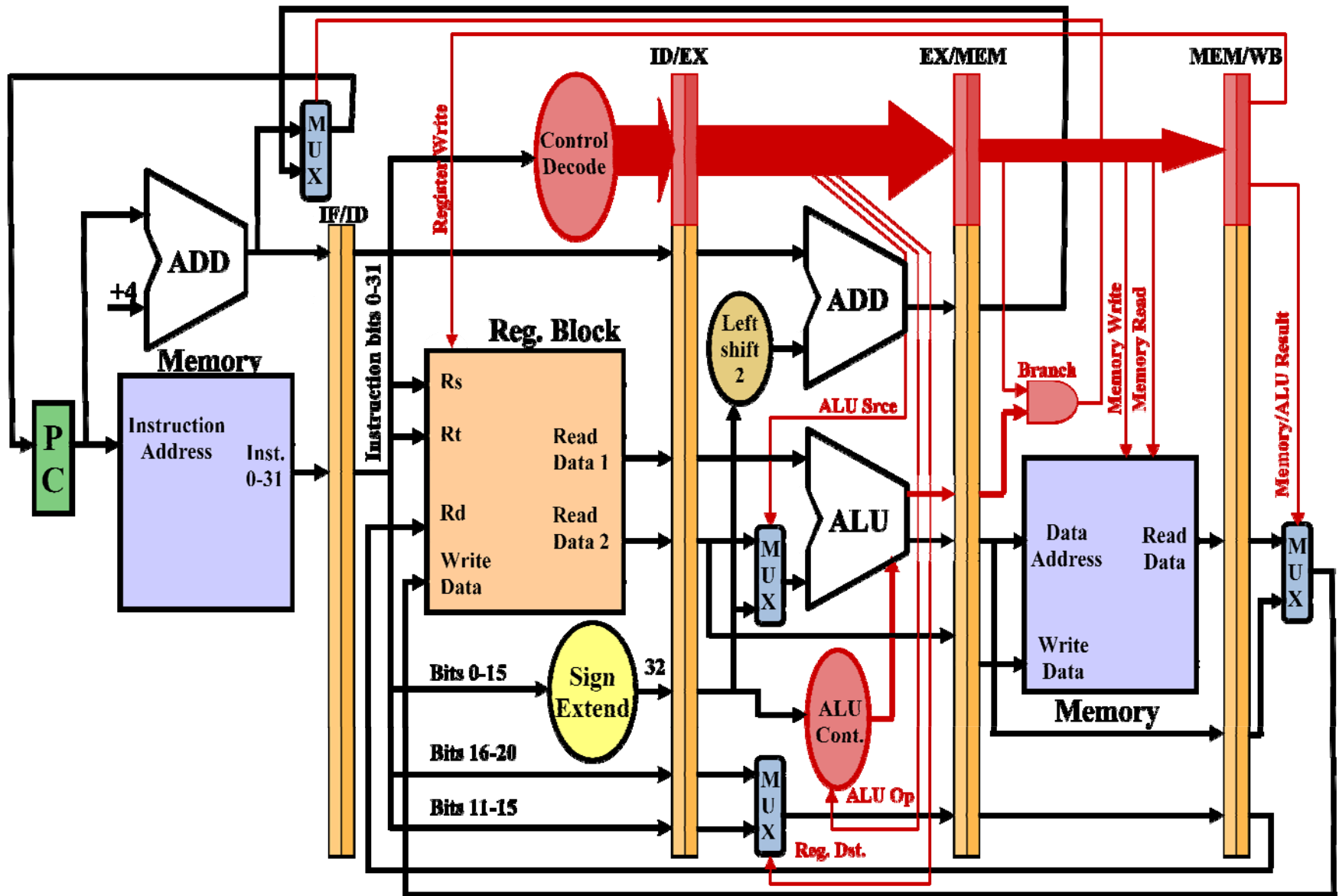
- Using diagrams from Lecture 21 slides 20-30 as a guide to the information to provide, show the data flow of `lw $t0,256($s2)` through the pipeline. Ignore control lines. Remember: Contents of a register are shown with square brackets (e.g., contents of `$t2 = [$t2]`).



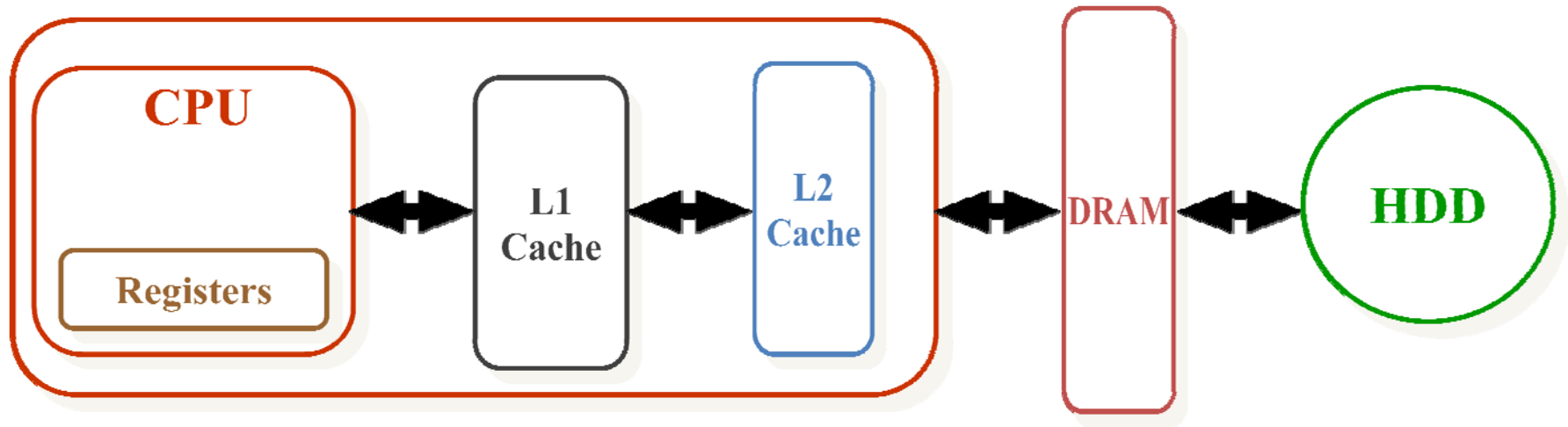
2. Show how `beq $t4,$t5,loop2`, if `loop2` is 40 instructions farther up in memory from the next instruction, and the branch is taken. Ignore controls except for the branch bit flow.



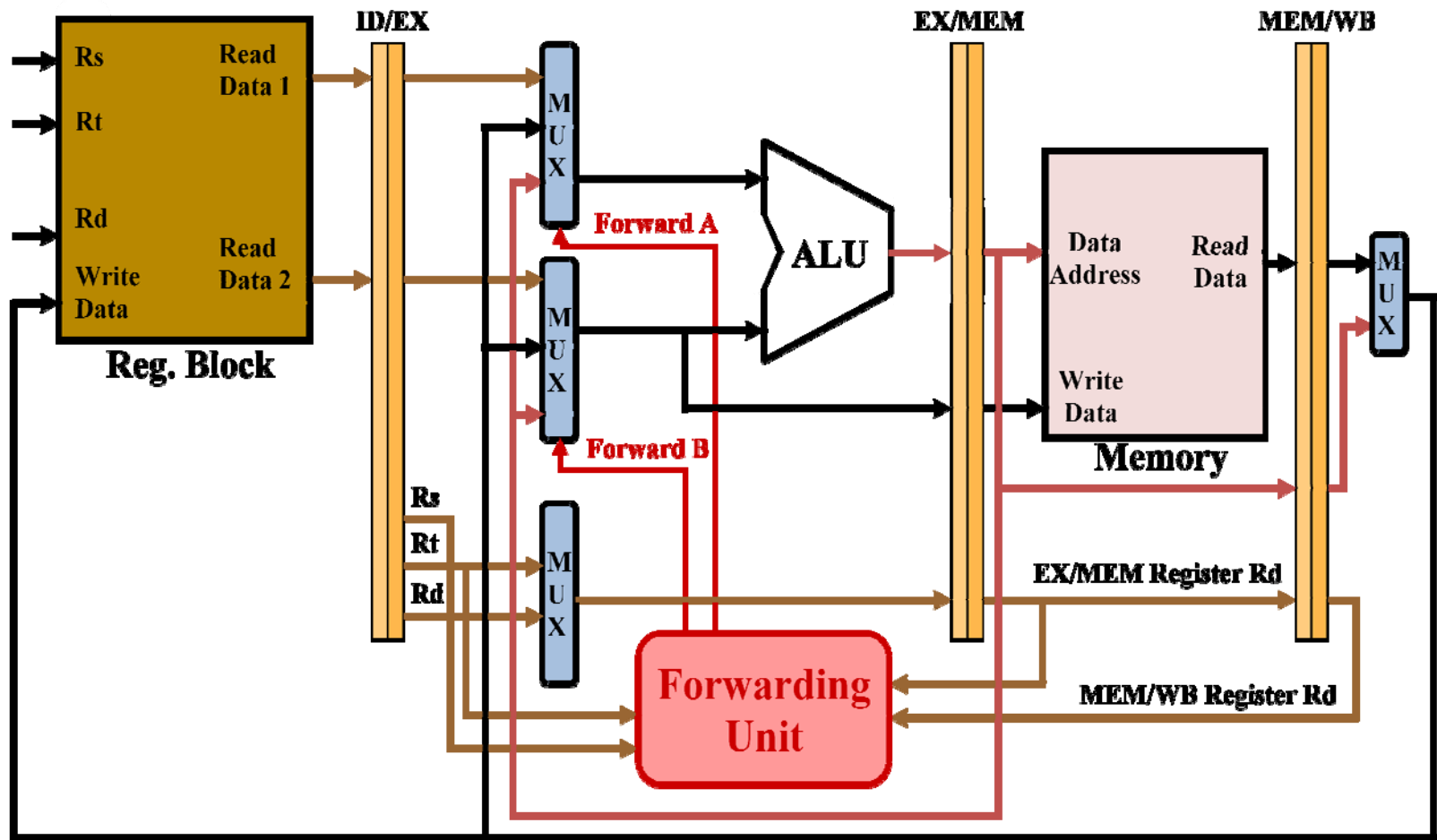
3. Show the pipeline progress of the instruction `add $t5,$t3,$t4`. If `$t3` holds `0x23` and `$t4` contains `0x1a9`, what hex number is on the ALU bypass bus?



4. Show how and \$t0,\$t1,\$t2 data travels through the pipeline (ignore control lines except for the register identification bus). If \$t1 contains 0x 10010023 and \$t2 contains 0x ffff, what is the numerical value in hex of the data on the ALU bypass bus? Show this value in the diagram.

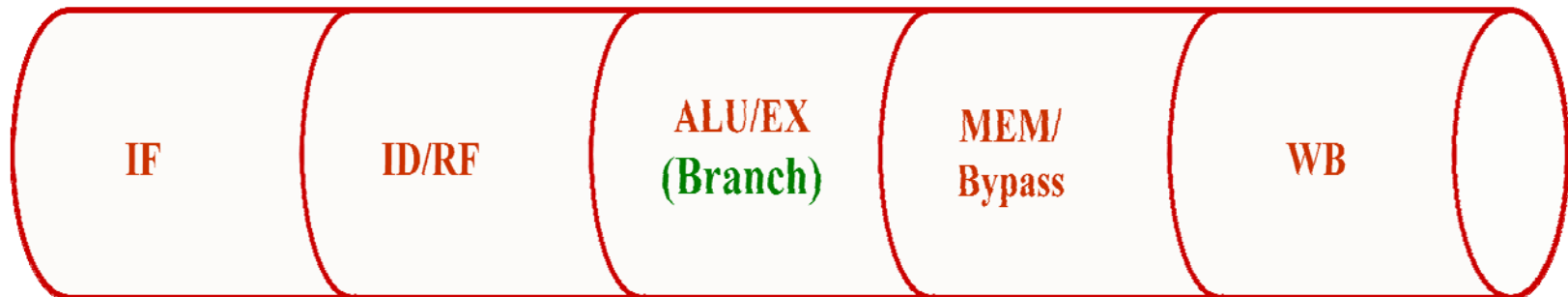


5. If the register access cycle (read or write) is approximately 100ps, show the approximate cycle time for the L1 and L2 cache and DRAM. What is the average HDD cycle in ms?



6. In the forwarding unit above, if Read Data 2 is from \$t0 and the data on the ALU bypass bus is from the instruction add \$t0,\$t1,\$t2, show the data flow that results in the correct register data arriving at the lower ALU data input.

# MIPS R-2000 Pipeline Processor



7. Assume you want to add a branch history unit to the pipeline to improve branch prediction. Draw it as a box affixed to the pipeline stage where it would go, and show a circuit connection to the stage where the branch history data is directed.