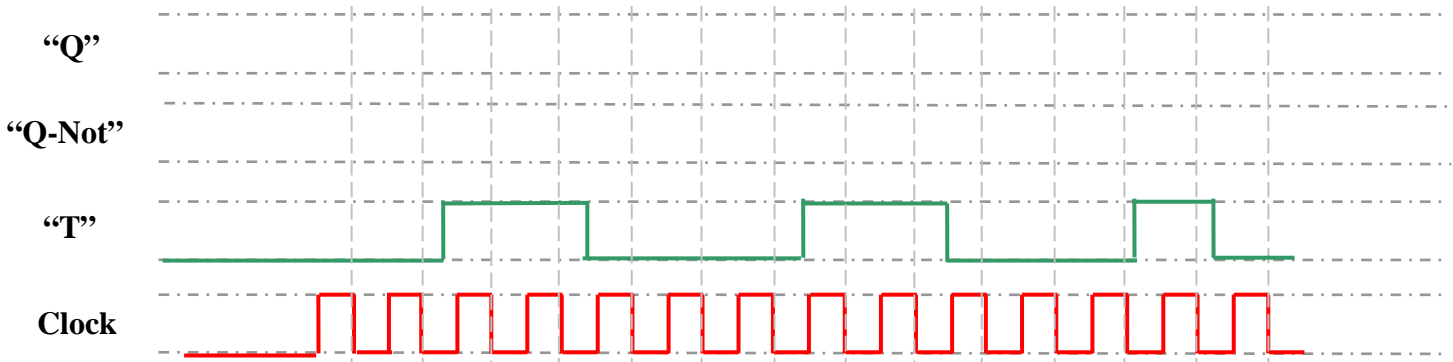
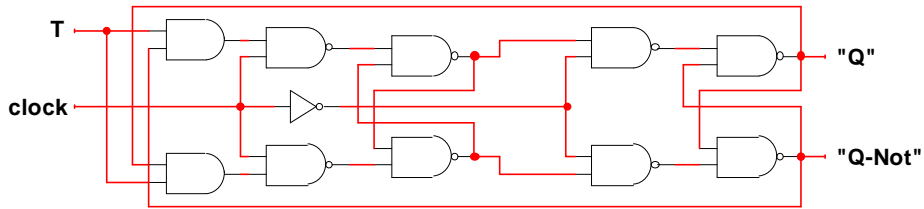


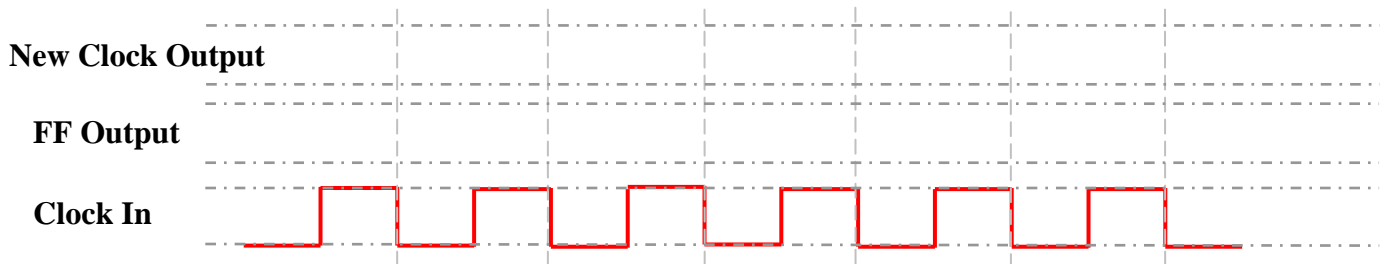
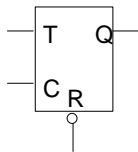
EE 2310 Homework #4 – Complex Flip Flops and Sequential Logic

Name _____

- The FF shown is a master-slave T FF. The clock is shown below in the timing diagram, and the T input is activated as shown. Assume that the flip-flop is initially in the Reset state. Then plot Q and Q-Not for the number of clock pulses shown.



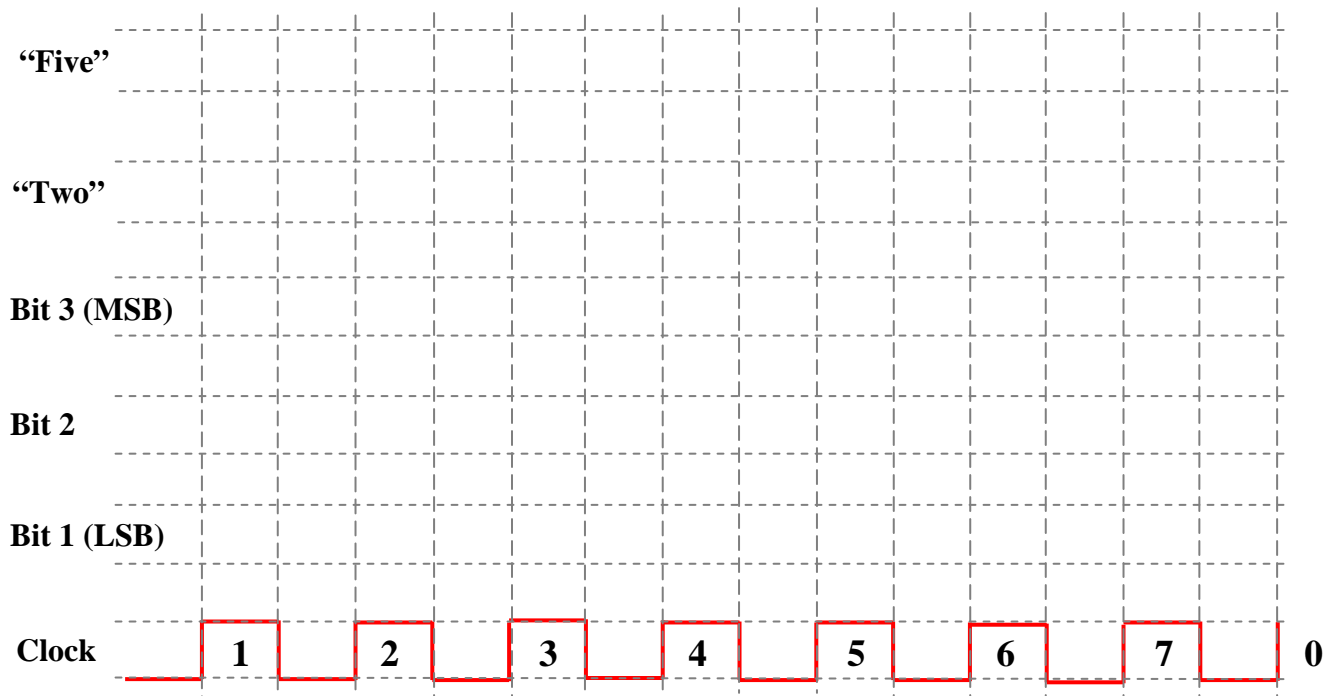
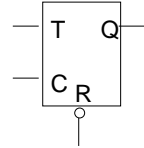
- Using the T FF shown below, devise a circuit that takes a 50-50 clock input and changes it into a clock output at $\frac{1}{2}$ the frequency that is a 25%-75% clock (i.e., it is logic 1 for one quarter of the clock cycle and 0 for three quarters of the cycle). Also, show the timing below. Note 1: leave the R (reset) line on the T FF unconnected. Note 2: All T FF's are master-slave.



Timing of New Clock at $\frac{1}{2} f$ and with 25-75 Duty Cycle

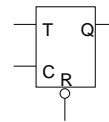
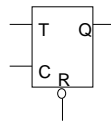
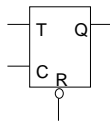
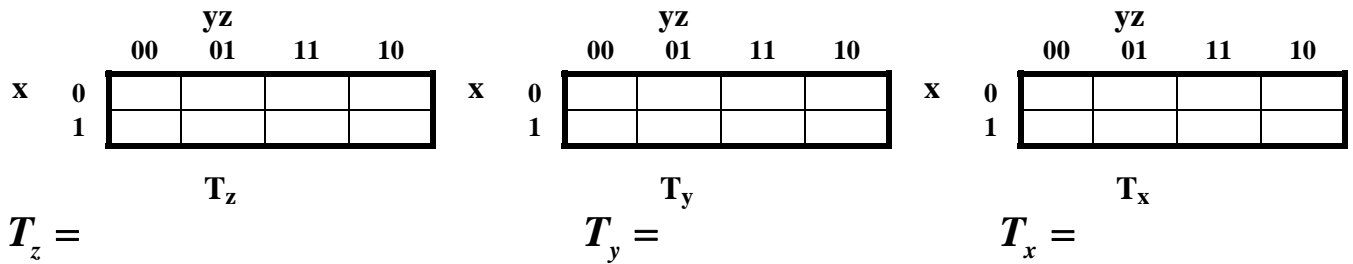
3. A three-bit synchronous (parallel) counter is to be constructed, and two events decoded from its output. The binary numbers 2 and 5 are to be decoded, ANDed with the inverted clock pulse, and transmitted to another circuit. Thus signals “2” and “5” last $\frac{1}{2}$ clock cycle, after the counter outputs are true; i.e., they are true when clock is false or low. The counter is free-running, and is only cleared at start-up by a common reset pulse tied to all the ff reset inputs. In summary:

- Counter inputs are clock and reset
- Counter outputs are signals “2” and “5”
- Input signals come from the left, output signals exit to the right
- Use the T ff shown to the right, and show the timing diagram on the form below.



Timing of Decoded Pulses

4. Construct a modulo-7 parallel (synchronous) counter from the three T master-slave FF's shown below. That is, the counter should count up to six, and reset to zero on the seventh pulse. Call the stages of the counter x, y, and z. The T-inputs of the stages are then T_x , T_y , and T_z . Remember that for each ff to toggle when the clock input cycles, the T input must be set to logical "1." Construct a timing diagram for clock and the three "Q" outputs of the counter on the chart below. Use either the Karnaugh map method or the "short-cut" method to design the counter. Since the counter flip-flops are master-slave, all outputs change on the down-going or "backside" edge of the clock.



Timing of Modulo-7 Counter

5. A “ring” counter is a shift register with one or more bits set to one and the rest set to 0. The last-stage output of the shift register is connected to the first stage, so that the 1’s are passed through the shift register, circulating through all the stages in sequence, in what can be regarded as a “ring” of flip-flops whose every output is connected to the next input. If one stage of the shift register is arbitrarily selected as “output,” this output stage will output only 0’s for (n-1) cycles, but a 1 every nth cycle, so that it functions as a counter with frequency 1/n, where n is the clock frequency.

More than one of the flip-flops can be set to 1, however, and then the ring counter can become a pulse or signal generator with a more complex cycle. From the five master-slave D-FFs below, construct a “ring” counter with the following more complex cycle: Assume that the ff’s 1 and 4 will be set after the clear pulse on startup. After the set and clear pulses shown on the timing diagram, the clock starts and the counter runs continually. Show the rest of the timing of the output for the number of clock cycles indicated below. Note: make sure you connect “Clear” to all the counter stage resets and “Set” to bits 1 and 4. Assume the serial timer pulse output is from FF #5.

