

EE 2310 Homework #3 – Simple Flip Flops and Timing Diagrams

Name _____

Simple RS-Flip-Flops can be made from any two 2-input combinational logic gates plus some inverters. Design the following RS flip-flops, labeling S, R, Q, Q-Not (and clock, as necessary). Make sure you label the polarity of R and S when active as well (+ or –).

1. Two AND gates plus inverters as needed.
2. Two OR gates plus inverters as needed.
3. An OR and an AND plus inverters as needed.
4. A NOR and a NAND plus inverters as needed.

5. Construct a clocked RS flip-flop using only NOR gates and inverters.

6. Given a clocked RS flip-flop, show the output Q versus clock, Set, and Reset as shown below. Note: Set and Reset are active high (+).

