

EE 2310 Homework #8 – MIPS Architecture Questions

Name: _____ Student Number: _____

Below are a set of questions that come primarily from Lectures 17 through 22 (although a few may be from other lectures). Answers will not be posted. However, five of these questions will be on the final exam (worth 3 points each for a total of 15 points). Find the answers to these questions and make sure they are on your “cheat sheet” – they will be worth 15 points on the final.

1. The instruction pair used to call and return from procedures are:
2. Where is the stack? In what direction does it grow?
3. Is the stack “LIFO” or FIFO?”
4. The stack pointer is what register number and what is its symbol?
5. A reserved section on the stack for a procedure or some other function is called a _____?
6. Is the following true or false? The s-registers must be protected by the calling program and the t-registers by the called program.

7. True or false: Windows is an application program that runs under Unix.
8. In a multiprogramming environment, what does “simultaneous” mean?
9. What is the difference in a program and a process?
10. What is a process switch?
11. What is an exception?
12. Define the computer ALU.
13. Define the computer control unit.

14. What is the 32-bit ALU made up of?

15. What do we really mean by references to “instruction memory” and “data memory,” since all memory is the same?

16. How many registers are there in the MIPS register block?

17. What does the sign extender do?

18. Why and how is the ALU used in data memory access instructions?

19. Name any two places in the single-cycle ALU where multiplexers are used.

20. Explain how the multicycle implementation speeds up the MIPS CPU.

21. How is the MIPS pipeline different from the multicycle design?

22. Name the five parts of the multicycle implementation (which have the same names as the five sections of the MIPS R-2000 pipeline).

23. Why are intermediate results registers required in the MIPS pipeline implementation?

24. What are the acronyms for the interfaces between the pipeline sections?

25. When is the ALU bypass bus used?

26. What is a data hazard in the MIPS pipeline?

27. What is a control hazard in the MIPS pipeline?

28. How can a forwarding unit prevent both data and control hazards?

29. Why does the forwarding unit not always work?

30. How is this problem overcome by stalling?

31. What is the latency in a hard disk drive?

32. True or false: Cache memory, or static RAM, is composed of flip-flops. Dynamic random access memory (or DRAM) is a much simpler electronic memory with only one transistor per cell.

33. True or false: Hierarchical memory management and cache memories result in an environment where each application appears to have the full range of memory.

34. Arrange the following memory devices in order, from fastest to slowest:

Hard disk, L1 cache, DRAM, L2 cache, CPU registers

35. True or false: Modern DRAM memories are much faster than state-of-the-art CPU chips such as the AMD or Intel processors.