Fall 2008, CS 4341.501, Digital Logic and Computer Design

Project

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Due BEFORE class on Monday, November 17, 2008

In this project you will design a specific hardware system, an ALSU, from fundamental principles. The approach should be to design the first level building blocks from gates. The second and succeeding level building blocks should be developed with the help of lower level building blocks. Think of the gates as the zeroth level building blocks. In each case, the inputs, outputs, timing, and functions of each of the used and developed (or being developed) building blocks must be clear. With this approach, the bigger functional blocks will not look cluttered.

Data words will be 16 bits long. The ALSU will have 16 microoperations, exactly one of which will be active during any time. Let B and/or A be the generic name/s of the input operand/s to the ALSU. The arithmetic operations are in 2's complement notation. The entire ALSU is a combinational system. The C_{in} comes in from outside. There are four status flags which are functions of the result of the current ALSU operations. They are the V for overflow, Z which should be 1 if the result turns out to be all zero bits, C, which is the Carry out of the sign position, and S, the sign bit of the result. These four lines are additional output lines. Following are the ALSU operations.

Serial number	Acronym	Function	Comment	Flags
1	TRA	A	Output A	ZS
2	ADD	$A + B$		$VCZS$
3	NEG	$-B$	Output negative of B	$VCZS$
4	SUB	$A - B$		$VCZS$
5	INC	$A + 1$	unsigned	ZS
6	DEC	$A - 1$	unsigned	ZS
7	SHR	Logic Shift Right $0, A$	with 0 shifted in	CZS
8	DIV	$\frac{A}{2}$		CZS
9	MPY	$A \times 2$		VCZS
10	SHL	Logic Shift Left $A, 0$	with zero shifted in	CZS
11	SLC	Shift left A, C_{in}	with C_{in}	CZS
12	SHR	Shift right C_{in}, A	with C_{in}	CZS
13	AND	$A \cdot B$	bit by bit AND	ZS
14	IOR	$A + B$	bit by bit OR	ZS
15	INV	$\overline{A}$		ZS
16	NOP	Hi-impedance	Release output bus	