

CS 4341.501 Midterm 1. Fall 2008

Guidelines

Question 1; 10 points

Design a two input Ex-OR circuit with the help of NAND gates only. You can use any number of NAND gates (no need to minimize anything).

$$a \oplus b = \bar{a}b + a\bar{b} = \overline{\overline{\bar{a}b} \overline{a\bar{b}}}$$

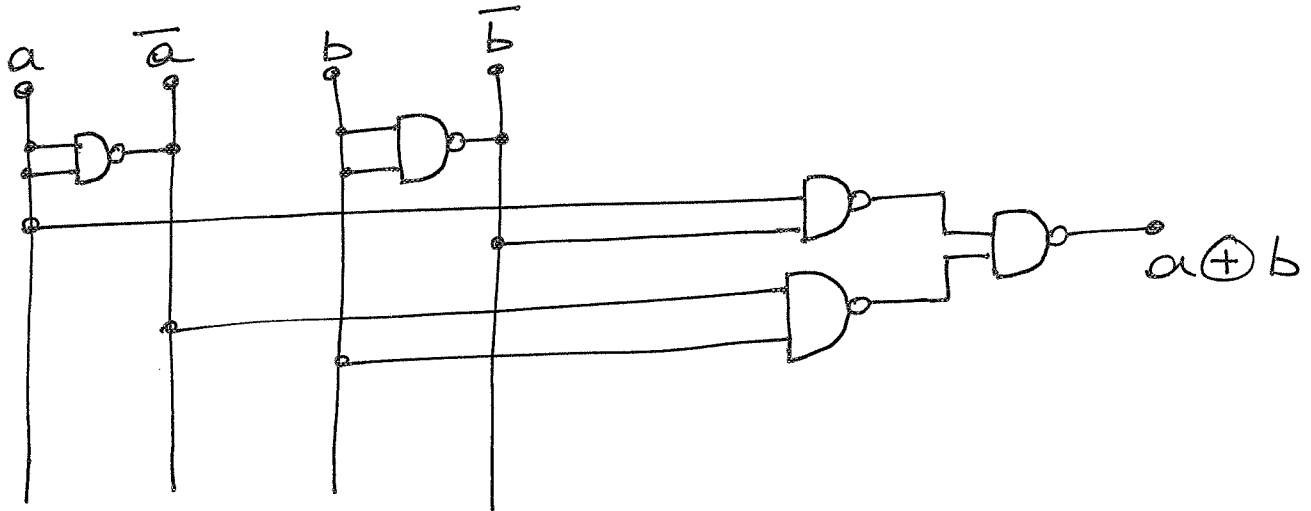


Table 1: Boolean function for Question 2

a	b	c	$f(a,b,c)$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Question 2; 10 points

Design a logic circuit for the Boolean function given in Table 1. The circuit should use an 8 input-line multiplexer (and a few other gates, only if necessary).

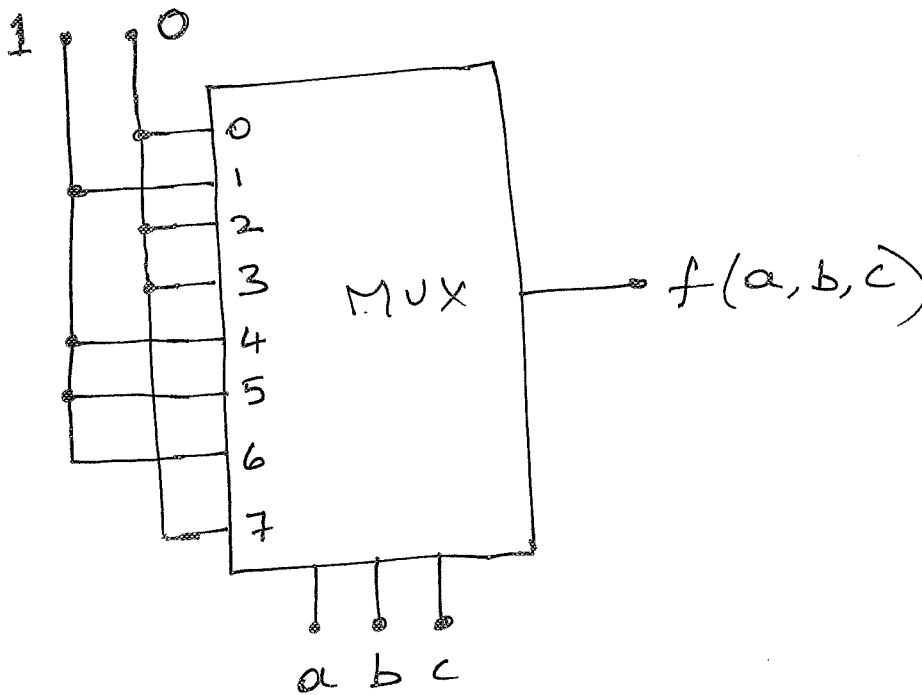


Table 2: K-map for Question 3

	$\bar{c}\bar{d}$	$\bar{c}d$	cd	$c\bar{d}$
$\bar{a}\bar{b}$	1	1	x	x
$\bar{a}b$	1	x		x
ab		x	x	x
$a\bar{b}$		1	1	1

Question 3; 25 points

For the function entered on the K-map above in Table 2,

1. Group and list all the essential prime implicants (5 points).
2. Give a minimized SOP expression (15 points).
3. How many don't care elements map to 1 in your minimized SOP (5 points)?

- ① All the prime implicants are grouped in the above figure. There is no essential prime implicant.
- ② A minimized SOP expression: $\bar{a}\bar{c} + ad + ac$
- ③ Number of don't care entries the above minimized expression that map to 1 is 4

Question 4; 15 points

Design the internal details of a PLA that has two input lines a and b . The PLA has two output lines f and g . The two functions implemented by the PLA are

$$f(a,b,c) = a \oplus b = \bar{a}b + a\bar{b} \quad (1)$$

$$g(a,b,c) = a + b \quad (2)$$

Note that $a + b = (a \oplus b) + ab$.

We can generate both the functions with three product terms. There are other ways. Any PLA approach that ~~correctly~~ generates correct function will get points.

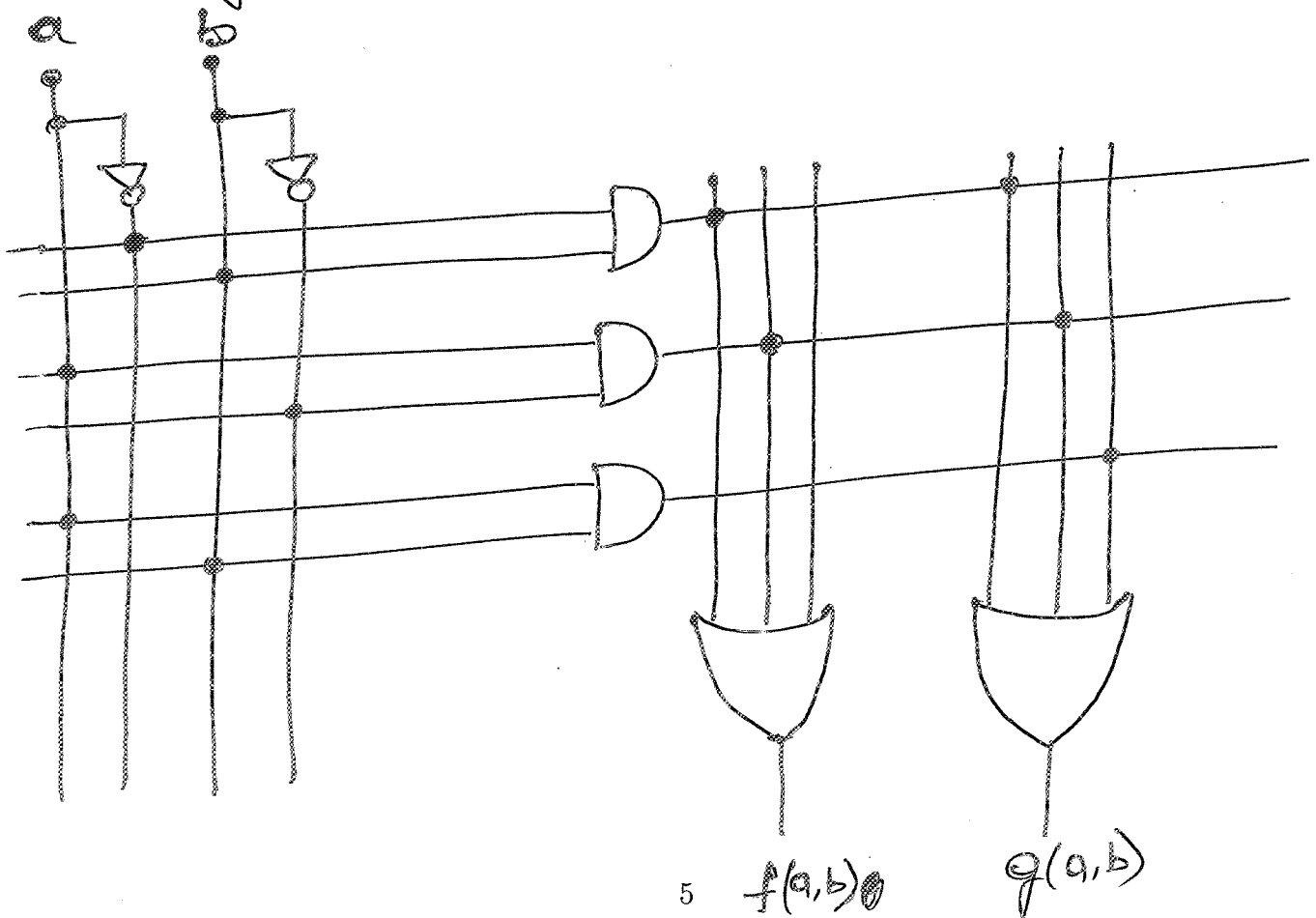


Table 3: Characteristics of the NOR latch. Figure 1. Logic circuit for the NOR latch

a	b	c	d
0	0	0	1
0	0	1	0
0	1	1	0
1	0	0	1
1	1	Don't	use

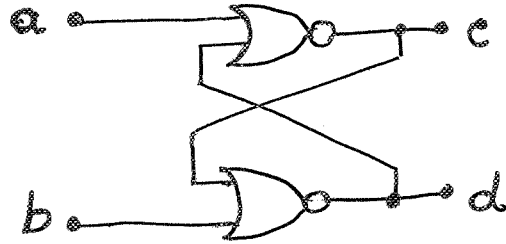


Table 4: Input-output sequence as a function of time

t	0	1	2	3	4	5	6	7
a, b	01	00	10	01	00	01	10	10
c, d	10	10	01	10	10	10	01	01

Question 5; 15 points

Table 3 and the Figure show the characteristics and the logic circuit for a NOR latch. At the beginning of operation of the circuit (that is, at time $t = 0$ seconds), the two inputs are $a = 0$ and $b = 1$. After every second of time, the input lines are changed, as given in Table 4. Determine and enter (in Table 4) the outputs soon after each such change.