

**Fall 2008; CS 4341; Sections 002 and 501; Digital Logic and Computer Design; Solutions for HW 6**

1. How many data input buses does the Register file have? Specify a list of data sources for each of them.

**Answer**

One. The data sources for it are EPC, PC+4, ALUout, and RAMout

2. How many registers can we simultaneously address in the register file? What are their functions? Where do these register addresses come from?

**Answer**

Three.

Two of them produce outputs of two registers, at RD1 and RD2, respectively.

The addresses for each of these is input as a 5 bit bit-pattern, at A1 and A2, respectively.

A1 and A2 are hardwire connected from the **rs** and **rt** fields of the instruction bit pattern.

The third of the registers that can be addressed in the register file selects one as a destination for data input to the register file.

Its 5 bit address bit-pattern is input at A3 of the register file. A3 is multiplexed from **rt**, **rd**, and a constant bit pattern (for **\$ra**). Of course, **rt** and **rd** are the fields of the instruction bit pattern.

The data input to the register file is input at WD3. The data for this is multiplexed from EPC, PC+4, ALUout, and RAMout.

3. How many different data words can the register file simultaneously produce? What are the different purposes of these outputs?

**Answer**

Two.

The first output originates from **rs** and it is hardwire connected to the first operand of the ALU.

The second output originates from **rt**. This is sometimes (sometimes, through multiplexing) used as the second operand to the ALU. This is also used as the input to data RAM.

4. List the different sources for each data input to the ALU.

**Answer**

The first operand originates from **rs** and it is hardwire connected to the ALU.

The second operand is multiplexed from **rt** or the extended Immediate operand.

In addition, the ALU needs the **shamt** field from the instruction bit pattern as another input filed.

5. List the different sources for the address input to the RAM.

**Answer**

There is only one source for the RAM address. It is the output of the ALU. The function the ALU should implement when RAM is addressed is the ADD. The operands the ALU should get for this function are `rs` and Sign Extended Immediate Operand.

6. List the different sources for the data input to the RAM.

**Answer**

Only one input source. The output of register `rt`, available at RD2 of the register file.

7. List the different destinations to which the data output from the RAM needs to reach.

**Answer**

Only one. The `rt` register in the register file.

8. How many different places does the input for the PC (Program counter) come from? What are they? What are their functions?

**Answer**

Five. These are PC+4, BTA, JTA, contents of register `rs`, or EHA (Exception handling address). If there is no exception, the address is selected from the first four of the five options, based on the MOPCODE and the status flags from the ALU. If the Exception status flag is on (1), EHA should be loaded into the PC.