

CS4341.002 (Honors) Midterm 1

Sept. 29, 2008

Guidelines

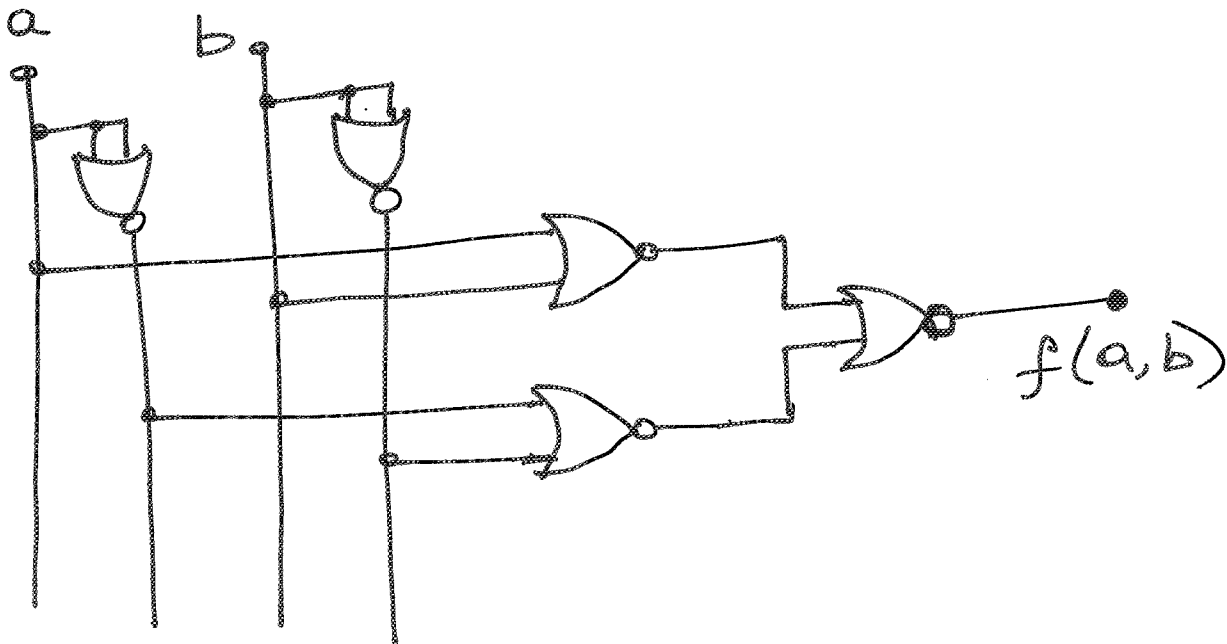
Question 1; 10 points

Design a two input Ex-OR circuit with the help of NOR gates only. You can use any number of NOR gates (no need to minimize anything).

A circuit with NOR is easier to implement starting from POS, which in turn is easy to obtain from \overline{f}

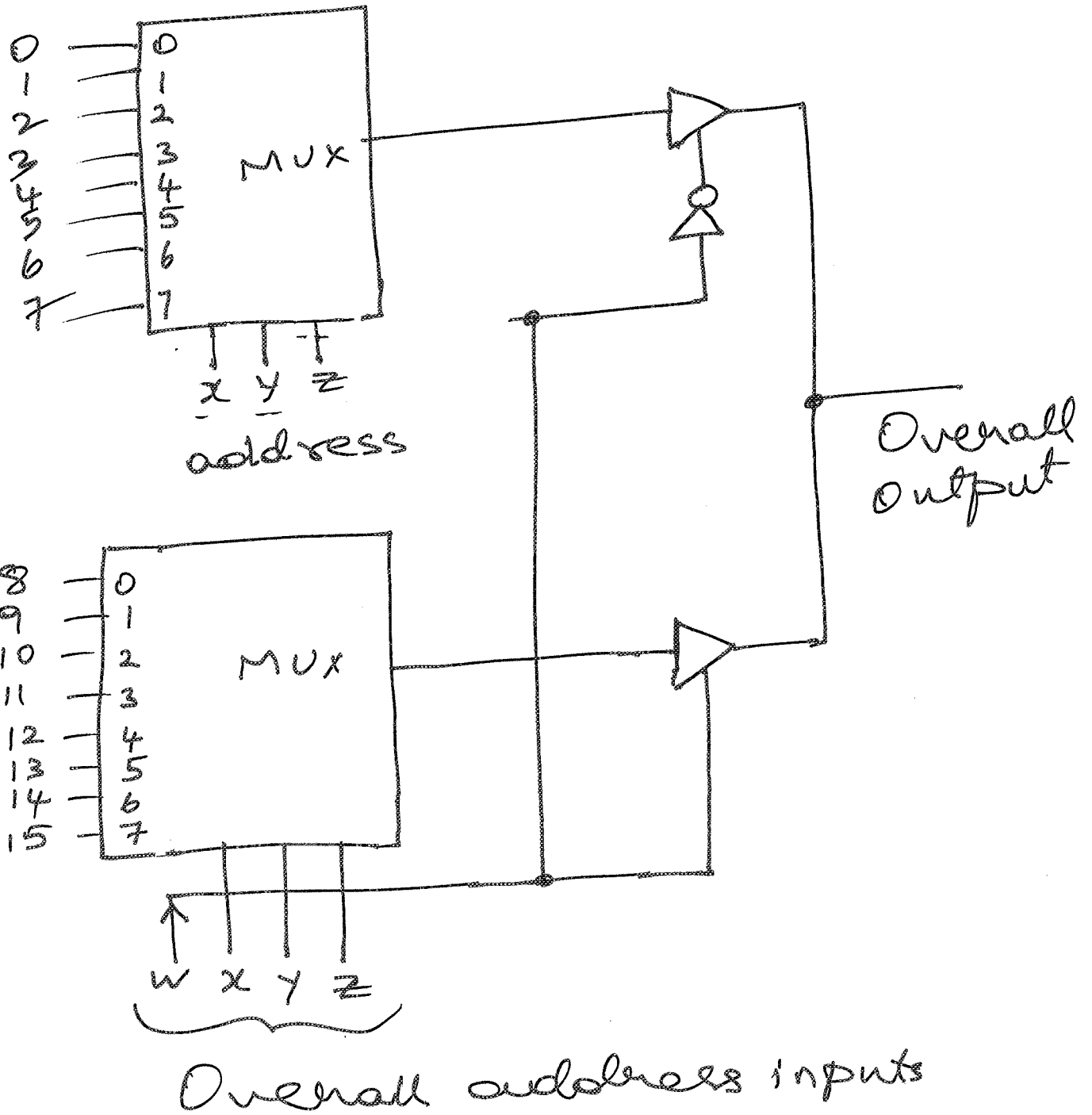
$$\overline{f(a,b)} = \overline{a \oplus b} = \overline{\overline{a} \overline{b} + ab} \rightarrow \text{from truth table \& sum of minterms}$$

$$\begin{aligned} f(a,b) &= \overline{\overline{a} \overline{b} + ab} \\ &= \overline{a + b} + \overline{\overline{a} + \overline{b}} \end{aligned}$$



Question 2; 15 points

Design a multiplexer with 16 data-input lines. You should use two multiplexers, each with 8 data-input lines. In addition, you can also use a few gates and tristate buffers.



Question 3; 20 points

Develop a minimized POS expression for the following function entered on the K-map. What is the number of 1 entries in the truth table of your final minimized expression?

	$\bar{c}\bar{d}$	$\bar{c}d$	cd	$c\bar{d}$
$\bar{a}\bar{b}$	1	1	1	1
$\bar{a}b$		x	1	x
ab			x	
$a\bar{b}$	1		x	1

$$\bar{f} = ad + b\bar{d}$$

$$f = (\bar{a} + \bar{d})(\bar{b} + d)$$

Looking at all the 1s & Xs outside the groups, we see that the expression has 8 minterms mapping to 1

Table 1: Characteristics of the NAND latch. Figure 1. Logic circuit for the NAND latch

s	r	q	p
0	0	Don't	Use
0	1	1	0
1	0	0	1
1	1	0	1
1	1	1	0

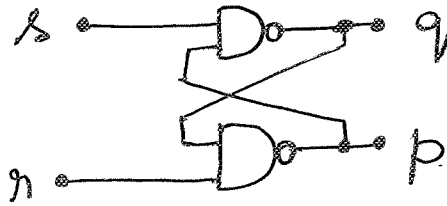
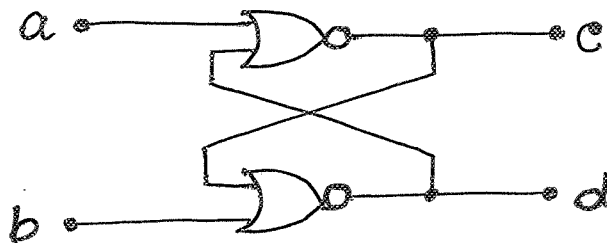


Table 2: Characteristics of the NOR latch. Figure 2. Logic circuit for the NOR latch

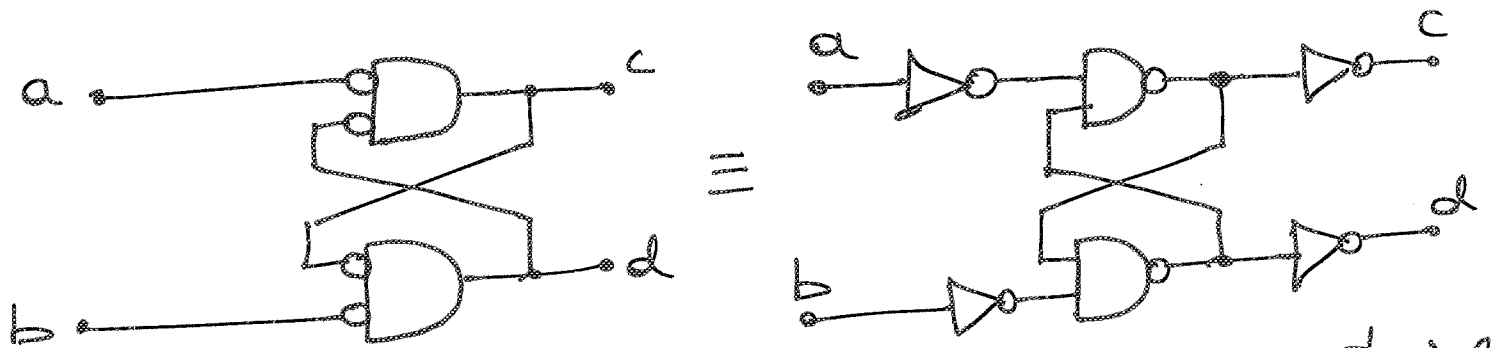
a	b	c	d
1	1	Don't	Use
1	0	0	1
0	1	1	0
0	0	1	0
0	0	0	1



Question 4; 15 points

Table 1 and Figure 1 above show the characteristics and the logic circuit for a NAND latch. In Figure 2, the NAND gates of the latch have been replaced by NOR gates. Determine the characteristics of the NOR latch and fill them in Table 2 above.

$\overline{a+d} = \overline{a} \overline{d}$ — Using this, modify the NOR latch to the equivalent

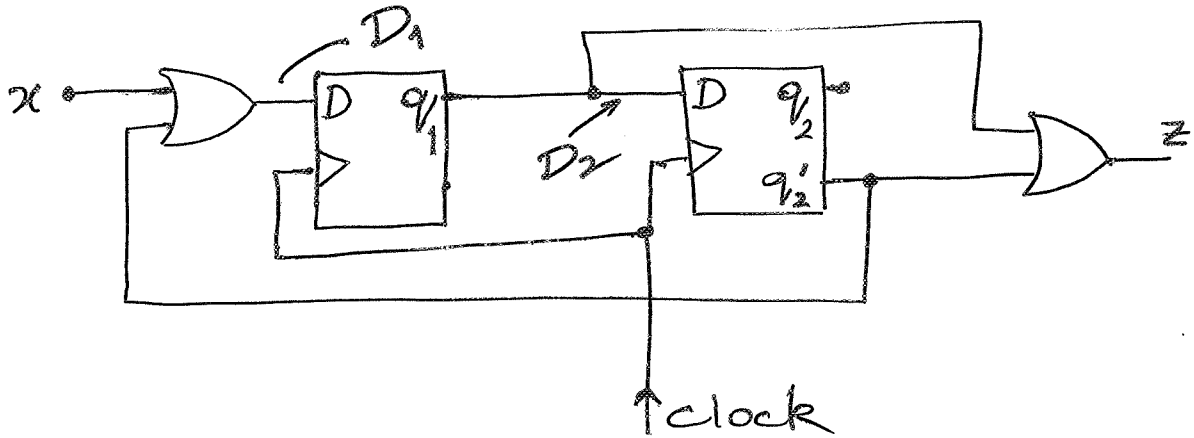


Now, fill in by modifying the entries in the NAND latch table.

Other methods are also fine.

Question 5; 15 points

Develop the state table for the following sequential circuit. Use the given "template" table in any appropriate way. Make sure you fill it properly; avoid ambiguity.



$$D_1(t) = x(t) + \bar{q}_2(t)$$

$$D_2(t) = q_1(t)$$

$$z(t) = q_1(t) + \bar{q}_2(t)$$

q_1	q_2	x	$q_1(t+1)$	$q_2(t+1)$	$z(t)$
0	0	0	1	0	1
0	0	1	1	0	1
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	1	1	1	1
1	0	0			
1	0	0			
1	0	1			
1	0	1			
1	1	0			
1	1	0			
1	1	1			
1	1	1			

$$q_1(t+1) = x(t) + \bar{q}_2(t)$$

$$q_2(t+1) = q_1(t)$$

$$z(t) = q_1(t) + \bar{q}_2(t)$$

↑
Enter these in the state table