High-swing, high-drive CMOS buffer

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Abstract: The advent of analogue and hybrid VLSI circuits has created new requirements for the design of many previously known building blocks. For example, implementation of cascaded multilayer analogue/hybrid neural networks requires output drivers that can charge the large number of interconnecting lines, and remain stable in the presence of large capacitive loads. A CMOS high dynamic range, high-drive buffer suitable for driving large capacitive loads is presented in this paper. An area-efficient output stage has been used, with which a rail-to-rail drive capability into a 5000 pF load at 160 kHz is achieved. The circuit occupies only 110 mils^2 in a 3 μm technology. The output range is rail to rail for $R > 10$ kΩ. The buffer is capable of driving resistive loads down to 300 Ω with acceptable THD.

1 Introduction

CMOS OpAmps with low drive capability are used extensively in applications such as switched capacitor filters, and the procedures and tradeoffs in the design of these amplifiers have been more or less clear for some time [1]. There are numerous design examples in this category reported in the literature. With increasing circuit density, however, and growing interest in very large-scale analogue and mixed mode circuits, an analogue buffer with efficient die area utilisation and wide dynamic range constitutes a very useful building block. The design of such a high drive buffer generally entails different constraints and priorities from those of low power or general purpose CMOS OpAmps.

A high-drive amplifier is typically required to handle capacitive loads in excess of 1000 pF and resistive loads of 1 kΩ or less with acceptable slew rate, phase margin and total harmonic distortion. Quiescent current, dynamic range in both input and output, and die area consumption are some of the other main issues in the design of OpAmps.

In the past, many designs have been reported in the literature that utilise interesting schemes to solve some of the problems associated with MOS amplifiers. The issues of output swing [2, 5, 6, 8, 9], input swing [5, 8, 9], and high linearity [2–4, 8] have been studied, among others. Most of the reported designs, however, are general purpose OpAmps and, because of their large die area, may not be the best choice for output drivers in analogue VLSI. The closest to our specifications was the circuit of Wong and Salama [7]. Unfortunately, this design exhibits stability problems (noted also in Reference 9), which are related to the pseudoswitching mechanism employed in the design to increase slew rate.

To be suitable for large-scale analogue applications with potentially large fan out, a buffer is restricted by the strict requirements of small die area and having a dominant pole at the load. Efficiency requirements in these applications necessitate that I/O subsystems occupy only a small percentage of die area. This constraint becomes even more severe in applications where the number of output pins is large (e.g. multichip analogue neural networks [11, 12]). The reason for the second restriction (i.e. a load compensated circuit) is that many such applications put very large capacitive loads on the drivers of the output stages; loads that cannot always be reasonably upper bounded at the time of buffer design. In internally compensated buffers, either with or without pole splitting, a large C_L reduces the magnitude of the secondary pole and decreases the phase margin. A dominant pole supplied by the load guarantees that the performance of the system (timing) degrades gracefully with increasing fan out, and not catastrophically owing to stability problems. Such a graceful degradation is usually tolerable as long as the natural frequency associated with the load is large compared with those given by the dynamics of the overall system in which the buffer is embedded.

This paper presents an alternative buffer design for large-scale analogue/hybrid applications based on the above criteria. The choice of the input circuits (complementary differential) and output (push–pull) was dictated by the requirement for high dynamic range. The main contribution of this design is the intermediate stage and combining the stages in an area efficient fashion so that stable operation is possible over orders of magnitude of load capacitance. The intermediate stage keeps the circuit stable at lower capacitive loads, while allowing for load-dominant compensation, which is necessary for high capacitive loads. It also supplies a large swing to the

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gates of the output transistors so that, given a certain drive requirement, their area can be minimised. The buffer was implemented in a 3 μm double metal, single polysilicon p-well process and has a rail to rail input and output range for loads greater than 10 kΩ. It occupies less than 110 mils^2 of die area. In the following sections, a description of the circuit is given, and its performance analysed.

2 Circuit description

In a high-swing 5 V design, the choice of output stage is limited to the common source configuration. Although the source follower and its variants provide better frequency response characteristics, the gate-source voltage overhead imposed by MOS transistor threshold voltage puts a severe limitation on dynamic range in these configurations. Since larger output swing was a high priority in this design, a common source output stage was chosen.

The schematic of the buffer is shown in Fig. 1. The dimensons of the devices are given in Table 1. A complementary differential pair is used in the input stage to provide large input common mode range. The advantage of this configuration is that it provides gain in the regions near the power rails. It is also known to have the following two problems.

(i) In the regions near the rails, when one of the pairs is shut off, the common mode rejection ratio is low;

(ii) the transconductance of the stage is not constant. The slope of the transfer characteristics of this stage changes at $V_{DD} - V_{th}$ and $V_{SS} + V_{th}$.

Paroden and Degrauwe [9] presented a solution to this problem involving a coupling between the biasing circuits of the two pairs. The coupling circuit includes a linear resistor, difficult to implement in most CMOS technologies. Also, the corresponding increase in die area was found incompatible with our size constraints for an output buffer. Given that the problems mentioned above are not critical, and with consideration to the requirements outlined in the previous section, mainly the die area constraint, it was decided not to include the coupling circuit [9] in our design.

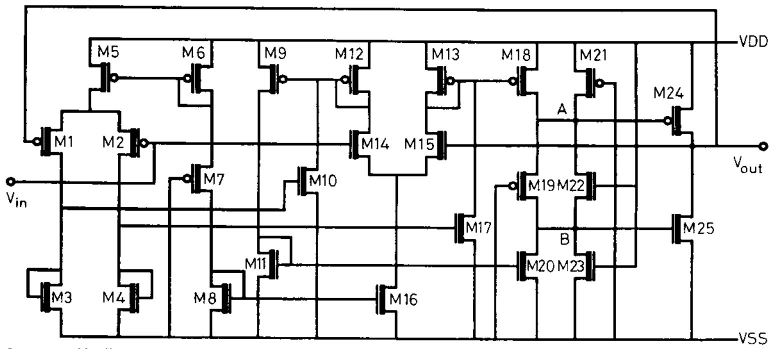

Fig. 1 *Schematic diagram of buffer amplifier*

Table 1 : Device dimensions

Device W/L dimensions			
	μm		
M1, 2, 14, 15	50.4/3	M11, M20	4.2/3
M3, M4	5.4/3	M19	3/9
M5, M16	5.4/3	M21	3/15
M6	7.2/3	M22	3/27
M7	3/6	M23	3/45
M8	6/6	M24	576/3
M9, 12, 13, 18	12/3	M25	252/3
M10, M17	15/3		

The output signal from the complementary differential pair is fed to an intermediate stage which does not contribute to the gain, but enhances the stability. Transistors M19 and M21–M23 operate in the linear mode and are basically used as resistors. These resistors reduce the impedance seen at the points A and B. Therefore, the poles produced by gate–drain capacitance of M24 and M25 will be shifted to a higher frequency. Since the pole produced by the load capacitance is now dominant, stability will be assured. A careful choice of W/L ratios for these devices results in stable operation and, at the same time, acceptable open loop gain and large voltage span at the gates of M24 and M25.

Because of large voltage variations at nodes A and B, transistors M19 and M22 are connected in a complementary configuration so that a linear I–V characteristic is maintained in the intermediate stage for the range of operations. Maintaining a symmetrical structure also reduces the second harmonic to a minimum and decreases THD considerably (see Figs. 5 and 6).

3 Performance analysis

The circuit was realised in a 3 μm single polysilicon double metal p-well process. The die photo is shown in Fig. 2. Die area, excluding the bonding pad area, is less than 110 mils^2. Maximum sinking and sourcing currents are 6.1 mA and 5.1 mA, respectively. With a load of 5000 pF, a down-going slew rate of 2 V/μs was obtained (Fig. 3). The quiescent current is only 165 μA.

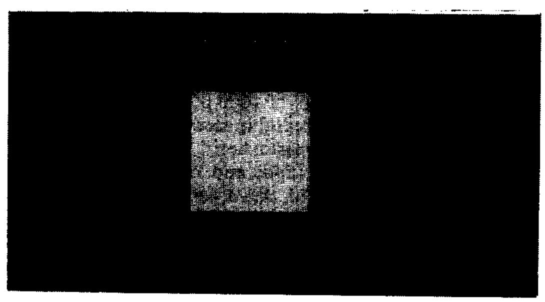

Fig. 2 *Die photo*

Table 2 gives the pole-zero configuration of the buffer in a variety of loads and biasing conditions. Variation of the frequency response and pole-zero location is a direct result of the output common source push–pull stage, the gain of which is dependent on the operating point. Despite these variations, however, the buffer maintains good performance in a wide span of load and biasing

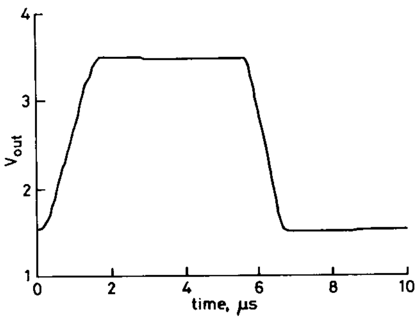

Fig. 3 *Output pulse response*
$C_L = 5000$ pF

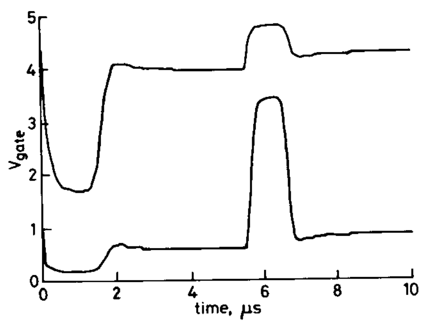

Fig. 4 *Gate voltages of output transistors M24 and M25 with same time axis as Fig. 3*
Simulated

conditions. A phase margin of 50 degrees or better is maintained for all conditions listed in Table 2. Note that other poles and zeros of the circuit that are not listed are at least 2.5 octaves away from those given, and hence have negligible effect on frequency characteristics.

With $C_L = 5000$ pF, all the poles are real. With $C_L = 200$ pF, the complex conjugate poles have a quality factor of $Q = 1.25$. For $C_L = 5000$ pF and a bias of $V_{in} = 4$ V, the third pole is a decade away from the complex conjugate poles, and the quality factor of the poles is $Q = 0.17$.

High die area consumption in many of the previous designs stems mainly from inefficient utilisation of output transistors (i.e. the voltage span on the gates of these

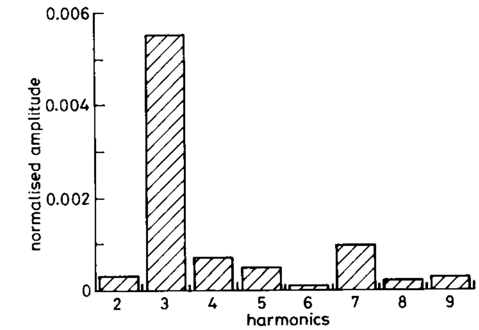

Fig. 5 *Normalised harmonics at 20 kHz for $R_L = 3$ kΩ*
Simulated

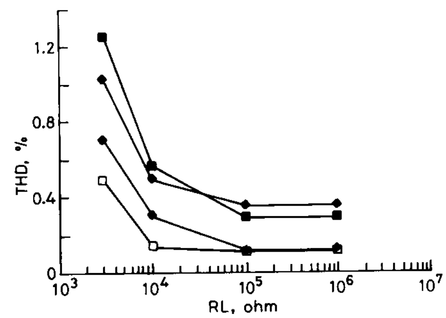

Fig. 6 *Total harmonic distortion against load resistance at 20 kHz and at different operating points*
Simulated; operating point
—□— 2.5 V
—◆— 3.0 V
—■— 3.5 V
—●— 4.0 V

transistors is small). Babanezhad [5], realising this problem, used a special output structure with a common mode feedback to increase the gate voltage span in output transistors. Once again, the added circuit would make the buffer too large for an output pad driver. In the circuit of Fig. 1, the voltage span of the nodes A and B is

Table 2: Pole-zero configuration in different loads and biasing conditions (simulated)

Load	Poles		Zeros	
	Real	Imaginary	Real	Imaginary
	rad/s		rad/s	
$C_L = 200$ pF	-5.386×10^6	1.469×10^7	-3.713×10^7	0
$R_L = 10$ kΩ	-5.386×10^6	-1.469×10^7	-1.531×10^8	0
$V_{in} = 2.5$ V	-3.938×10^7	0		
$C_L = 5000$ pF	-8.783×10^5	0	-3.684×10^7	0
$R_L = 10$ kΩ	-1.092×10^7	0	-1.533×10^8	0
$V_{in} = 2.5$ V	-4.027×10^7	0		
$C_L = 200$ pF	-5.409×10^5	2.426×10^7	-3.917×10^7	0
$R_L = 10$ kΩ	-5.409×10^5	-2.426×10^7	-9.486×10^7	0
$V_{in} = 4$ V	-3.866×10^6	0	-1.692×10^8	0
$C_L = 5000$ pF	-1.650×10^6	3.838×10^6	-3.156×10^7	0
$R_L = 10$ kΩ	-1.650×10^6	-3.838×10^6	-9.139×10^7	0
$V_{in} = 4$ V	-3.251×10^7	0	-1.602×10^8	0

more than 3 volts (Fig. 4) without added complexity. This is slightly lower than the gate voltage span [5], but it is achieved with a complexity that is many times smaller.

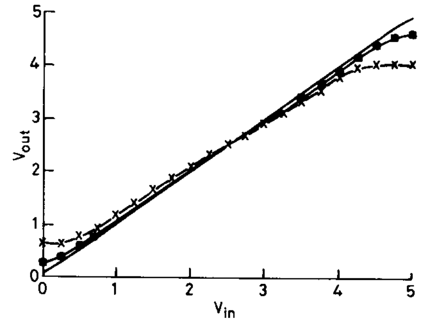

Fig. 7 *Transfer characteristics at various loads*
Load resistance
—— 10 k
—■— 1 k
—×— 300 k

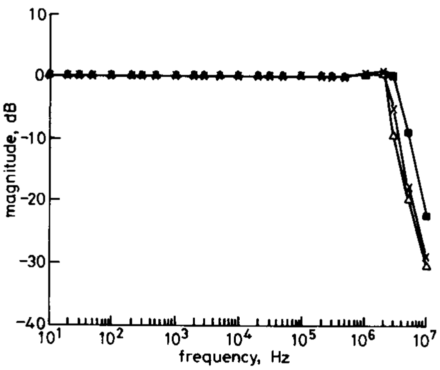

Fig. 8 *Magnitude response of buffer at different operating points*
$C_L = 400$ pF and $R_L = 10$ kΩ
—△— 0 V
—×— 1 V
—■— 2 V

As shown in Fig. 5, the second harmonic is very low, which is a result of the symmetrical structure of the amplifier. Total harmonic distortion with a 20 kHz input in a variety of load conditions are given in Fig. 6. Note that this is a worst case; THD is smaller in lower frequencies. The transfer characteristics and frequency response at various loads and operating points are given in Figs. 7 and 8. The buffer has a systematic offset of 0.54 mV and open loop gain of 43 dB.

4 Conclusion

A high-drive CMOS buffer with high dynamic range was introduced. The main criterion in this design was to achieve acceptable performance levels with a constraint on circuit size. The circuit occupies only 110 mils^2 and is therefore attractive for very large-scale applications. The buffer can drive a 5000 pF capacitor with a slew rate of up to 2 V/μs, but only dissipates 0.8 mW DC power, which is very small for a buffer with this drive capacity. The output settles in 2 μs for $C_L = 370$ pF. Tests and pole-zero configuration indicate stability in a variety of loads and biasing conditions. Rail-to-rail output swing is maintained down to $R_L = 10$ kΩ. With loads as low as 300 Ω, output swing is still 70% of the power supply and acceptable operation is possible in many applications.

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