

Conclusion: Preliminary experiments with an externally-modulated injection-locked diode array show no degradation

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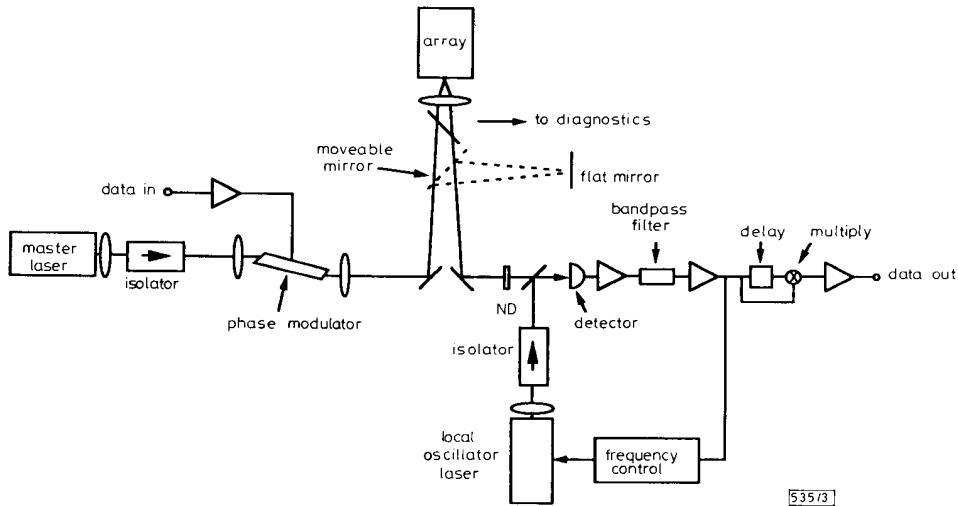


Fig. 3 Schematic diagram of heterodyne experimental apparatus

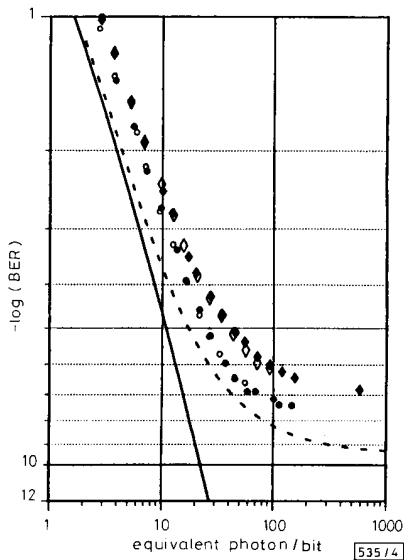


Fig. 4 Heterodyne results

- zero linewidth DPSK
- - - 15 MHz linewidth theory
- 2⁷ - 1 length PRS:
- ◇ baseline
- ◆ array
- Square wave:
- baseline
- array
- 1 Gbit/s data rate
- 15 MHz IF linewidth
- π modulation depth

in BER performance when compared to the performance of the same system with the array optically bypassed. The comparison was performed with a self-heterodyne configuration which eliminated the effects of laser linewidth and with a heterodyne configuration which was a more realistic approximation of a coherent communications link. Some pattern-dependent behaviour in the modulation/demodulation electronics is evident, independent of the array.

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HIGH-DRIVE CMOS BUFFER FOR LARGE CAPACITIVE LOADS

Indexing terms: Circuit design, Amplifiers

A new CMOS buffer circuit for high capacitive loads is presented. The objective of the design is a high-power, area-efficient buffer to be used in very large scale analogue applications. The buffer can deliver a slew rate of 1.2 V/μs to capacitive loads in excess of 5000 pF. It has a total harmonic distortion of less than 3% at 20 kHz. At stand by, it consumes only 125 μA (0.625 mW). The buffer occupies 100 mils² of die area in a 3 μm technology.

Introduction: The subject of opamp design using CMOS technology has been under study for some time. The design methodology and tradeoffs in cases with low, predetermined capacitive loads are well known.¹ This includes amplifiers

used in switched capacitor filtering and a variety of other applications where the amplifier has only to drive another circuit within the interior of the chip. Output buffers, however, should be able to handle large and sometimes variable capacitive loads from output pads, leads, IC pins, PCB wiring, and other loading at the output. Some examples of CMOS power amplifier design have appeared in the literature during the past few years.²⁻⁸

In addition to these requirements, if the buffer is to be used in a very large scale application, it should occupy a small portion of the chip. The application leading to this design is a multilayered analogue neural network where the number of output pins is relatively large. This application emphasises the need for buffers that consume a small portion of chip area and power. The available designs, with area consumptions of up to thousands of mils² are not suitable for this purpose.

In this Letter, a high-drive buffer for large capacitive loads is presented. The buffer operates on a single 5 V supply and occupies only 100 mils² of die area.

Circuit description: The schematic diagram of the circuit is given in Fig. 1. The transistors M1-M5 and M9-M13 form

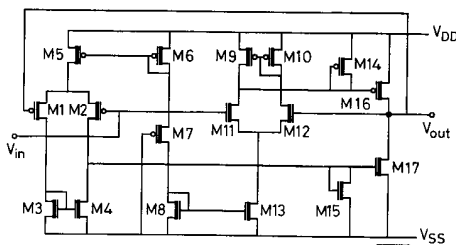


Fig. 1 Schematic diagram of buffer

two complementary differential stages. The inputs of these stages are connected in parallel. Each of them drives one half of the output common source push-pull stage. By using two input stages in parallel, the intermediate level-shifting stage, normally needed to feed a push-pull output stage, is eliminated. The drawback of this approach is that it slightly increases the harmonic distortion. This increase in distortion is tolerated for our applications; the alternative is to include compensation capacitors, which will significantly increase buffer area. Transistors M14 and M15 are connected as resistors. Their function is to decrease the impedance at the gates of output transistors M16 and M17 and act as frequency compensation capacitors.

Performance analysis: The pulse response of the buffer with a 5000 pF capacitive load is shown in Fig. 2. Slew rates of 1.2 V/ μ s and 0.5% settling time of 3 μ s have been achieved with this load. Fig. 3 shows the transfer characteristic of the buffer. Output voltage span is 94% of the supply range with a 5 k Ω load and rail to rail for $R_L > 10$ k Ω . Although the input circuitry is design in two half parts, total harmonic distortion is less than 3% at 20 kHz. Normalised harmonics of the input at this frequency for a 2 V peak to peak signal are given in Fig. 4; the quiescent current is only 125 μ A.

The frequency response of the buffer is shown in Fig. 5.

Dominant poles and zeros of the circuit are given in Table 1 for load conditions of

$$R_L = 10 \text{ k}\Omega \quad C_L = 500 \text{ pF}$$

$$R_L = 10 \text{ k}\Omega \quad C_L = 5000 \text{ pF}$$

In both cases, the moduli of the closest pole (zero) to those in the Table are at least 5 (3) octaves higher. With the 5000 pF load, the complex conjugate poles have a quality factor of

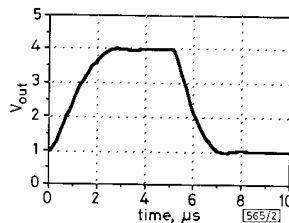


Fig. 2 Pulse response of buffer with capacitive load of $C_L = 5000$ pF

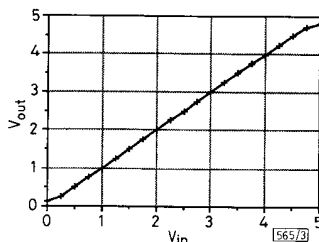


Fig. 3 Transfer characteristics with $R_L = 5$ k Ω

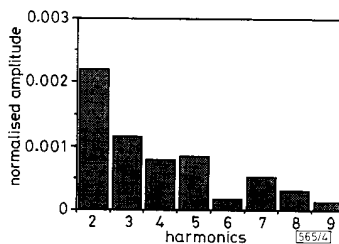


Fig. 4 Normalised harmonics of output at 20 kHz with $V_{in} = 2$ V peak to peak

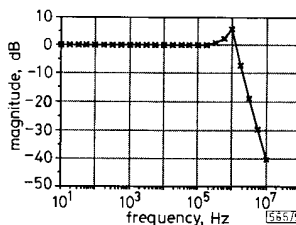


Fig. 5 Frequency response of buffer with $C_L = 5000$ pF, $R_L = 10$ k Ω

Table 1 POLE-ZERO CONFIGURATIONS

Load	Poles		Zeros	
	Real	Imaginary	Real	Imaginary
$C_L = 500$ pF	-1.344×10^6	1.991×10^7	-3.369×10^6	0
$R_L = 500$ pF	-1.344×10^6	-1.991×10^7	-1.467×10^8	0
	-3.369×10^6	0	-1.758×10^8	0
$C_L = 5000$ pF	-1.675×10^6	6.123×10^6	-3.369×10^6	0
$R_L = 10$ k Ω	-1.675×10^6	-6.123×10^6	-1.467×10^8	0
	-3.370×10^6	0	-1.758×10^8	0

$Q = 1.75$, and with $C_L = 500$ pF, $Q = 7.38$. The circuit operates acceptably over an order of magnitude variation of the capacitive load.

Summary: A CMOS buffer suitable for driving very large capacitive loads has been presented. The buffer is capable of driving 5000 pF loads with an output slew rate of 1.2 V/ μ s. The quiescent current is 125 μ A, and the THD is 3% at 20 kHz. The buffer occupies 100 mils² of die area and works acceptably over an order of magnitude variation in capacitive load.

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ULTRATHIN STACKED $\text{Si}_3\text{N}_4/\text{SiO}_2$ GATE DIELECTRICS PREPARED BY RAPID THERMAL PROCESSING

Indexing term: Dielectrics

Ultrathin (58 Å equivalent oxide thickness) stacked $\text{Si}_3\text{N}_4/\text{SiO}_2$ (NO) films with the bottom oxide prepared by rapid thermal oxidation (RTO) in O_2 and the top nitride deposited by rapid thermal processing chemical vapour deposition (RP-CVD) were fabricated and studied. Results show that the charge trapping and leakage current of the stacked films are comparable to those of pure SiO_2 and low-field breakdown events are significantly reduced. By scaling down the top nitride thickness the commonly observed flat-band voltage instability of MNOS devices was minimised, but the low-defect property was still preserved.

Stacked nitride/oxide (NO) films have received much attention recently due to their low defect density, low leakage current, diffusion barrier property, and excellent long-term reliability.^{1–3} However, efforts have been focused on using these dielectrics as storage dielectrics on either Si or polysilicon electrodes. The flatband voltage instability resulting from charge trapping in the nitride layer or at the nitride/oxide interface has limited the application of these films to memory elements.^{1,2,4} In this work, stacked NO films prepared by

rapid thermal processing (RTP) have been studied as a possible substitute of pure thermal SiO_2 for gate dielectric applications. The top nitride thickness has been scaled down to 30 Å such that charge trapping can be minimised. Results show that the stacked dielectrics exhibit comparable charge trapping and leakage current as compared with pure thermal SiO_2 of similar thickness, but have far fewer medium- and low-field breakdown events.^{2,3}

In this study, single-wafer RTP was used exclusively for gate dielectrics formation. The bottom oxide was prepared by RTO and the top nitride was deposited by RTP-CVD. These techniques allow high-temperature processing without an excessive thermal budget.

The starting materials were lightly boron-doped Si (100) substrates. The bottom oxide and the control oxide were both prepared by RTO in O_2 at 1050°C. The top nitride of the stacked NO dielectrics was deposited by using SiH_4 and NH_3 (flow rate ratio 1 : 40) diluted in N_2 . The deposition pressure was 1 torr and the temperature was 850°C. The nitride was deposited by an RTP-CVD system that uses tungsten-halogen lamps as the heat source. The nominal bottom oxide thickness was 40 Å and the top nitride thickness was 30 Å. No annealing or reoxidation was performed after top nitride formation. The dielectric thicknesses were all 'oxide-equivalent' and were derived by measuring the high-frequency (1 MHz) capacitances of MOS capacitors in the accumulation regime, assuming a dielectric constant of 3.9. LP-CVD polysilicon was deposited to a thickness of 4000 Å immediately after dielectric formation, followed by POCl_3 doping, photolithography and RIE. A forming gas anneal at 450°C concluded the device fabrication.

The capacitor I/V characteristics of both the control oxide and the stacked layers are plotted in Fig. 1. Stacked NO layers, especially reoxidised nitride/oxide layers (ONO) are known to exhibit lower leakage current as compared with pure oxide at high fields.⁴ Several factors contribute to the current reduction. The top and/or bottom oxides of stacked ONO and NO layers force electron conduction through the nitride, in which the electron mobility is now due to the presence of deep electron traps.⁴ Space charge at the nitride/oxide interface also reduces the electric fields at the carrier-injection electrodes, which further decreases the leakage current.⁴ In Fig. 1, however, the leakage current of the control oxide and the stacked nitride/oxide exhibits comparable leakage at low fields and the stacked layer shows even slightly higher current at high fields. The dark current in CVD Si_3N_4 has been found to increase with decreasing thickness at constant electric fields.^{5,6} The increase in conductivity has been attributed to diminished electron trapping in thin nitride films or to thickness fluctuation.^{5,6} In our case, the top nitride was very thin and consequently highly conductive. Such a thin top nitride cannot reduce leakage currents by charge trapping and is not resistant even to a reoxidation in dry oxygen at 1050°C for 30 s. As will be shown later, the advantage of adopting this thin top nitride is to reduce defect density while maintaining low charge trapping rates rather than reduce leakage current.

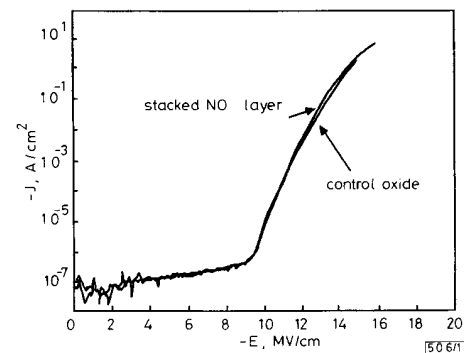


Fig. 1 Current density (J) against electric field (E) of pure SiO_2 and stacked NO layers

Electric field is calculated in terms of oxide-equivalent thickness